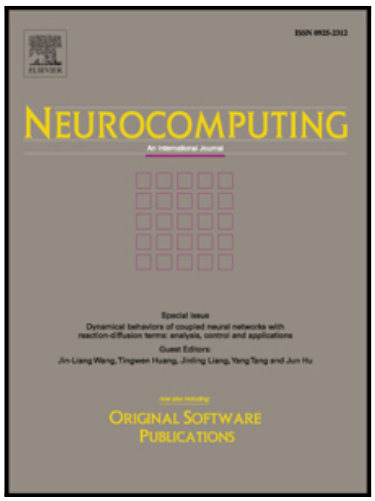

Fan-In Analysis of a Leaky Integrator Circuit Using Charge Transfer Synapses

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Fan-In Analysis of a Leaky Integrator Circuit Using Charge Transfer Synapses

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Abstract— **It is shown that a simple leaky integrator (LI) circuit operating in a dynamic mode can allow spatial and temporal summation of weighted synaptic outputs. The circuit incorporates a current mirror configuration to sum charge packets released from charge transfer synapses and an n-channel MOSFET, operating in subthreshold, serves to implement a leakage capability, which sets the decay time for the postsynaptic response. The focus of the paper is to develop an analytical model for fan-in and validate the model against simulation and experimental results obtained from a prototype chip fabricated in the AMS 0.35µm mixed signal CMOS technology. We show that the model predicts the theoretical limit on fan-in, relates the magnitude of the postsynaptic response to weighted synaptic inputs and captures the transient response of the LI when stimulated with spike inputs.**

***Index Terms*—neuromorphic circuits, fan-in, spiking neural network, leaky integrator, charge transfer synapse, CMOS**

1. Introduction

SPIKING NEURAL NETWORKS (SNN) implemented in hardware are an increasingly popular area, both in research and in commercial settings. Spiking neurons encode information in the timing of single spikes, and not just in their statistical firing rate [1]. Recent neuroscience research has shown that SNNs mimic neuron behaviour on a level more closely related to biology and so have the propensity for powerful computational ability compared to classic artificial neural networks.

Artificial spiking neural networks can be implemented with either software or hardware approaches. Several software simulators [2] have been developed to simulate SNNs and allow investigation of the role played by spike-timing in the field of computational neuroscience. However, software simulations with general-purpose platforms require high computational cost with no guarantee of real-time performance. Even the latest supercomputer to date has not shown capability for achieving real-time and detailed simulations for a large-scale SNN over multiple cortical areas. Several computational systems based on FPGAs, GPUs and ARM processor cores [3–5] have been developed for hardware accelerated simulation which could offer such capability at the expense of large silicon area and low energy efficiency.

Implementing SNN with dedicated hardware however, has a number of important advantages over software solutions. The major advantage is high speed computation with inherent high parallelism and distributed computing ability. There has been extensive activity in the development of hardware SNN including digital, analogue and hybrid implementations. Good reviews of the current progress of hardware SNN development can be found in [6–8]. Different neuron models have been used in current hardware SNN projects, varying from very detailed conductance-based models to simpler leaky integrate and fire versions. Conductance-based models emulate biophysical ion channels and hence are more faithful to biology. The integrate and fire models are less realistic but require fewer transistors. Their compact layouts and low energy consumption allow designers to balance the accuracy with a higher number of neurons in the network and hence are more scalable. Each of the different implementations offers some trade-off between scalability, latency and biological realism. Finding an appropriate balance between these three elements represents one of the key challenges of hardware SNNs.

This paper describes the dynamics of a leaky integrator (LI) circuit that aggregates the output of multiple charge transfer synapses (CTS). The LI is verified using simulation/experimental results and an analytical model is developed to relate the postsynaptic response to the fan-in, n. The remainder of this paper is organized as follows. Section II presents a comparison between digital and analogue hardware approaches to SNN implementation while section III presents a description of the operation of the CTS. Section IV details the fan-in model for two distinctly different operating conditions while section V presents both experimental and simulations results to support the model. Section VI presents a discussion of the work followed by a conclusion in section VII. Derivations of equations and details of processing can be found in the appendices.

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