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Thermal-Aware Network-on-Chips: Single- and Cross-Layered Approaches

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Abstract—In the era of the billion transistors on a chip that are capable of implementing thousands of processing cores, Network-on-Chips (NoCs) are the most viable and scalable solution to connect this massive number of cores. NoCs gradually support manycore processors technology, from conventional ICs with tens to hundreds of cores to 3D integrated ones with even more cores. On the other hand, many challenges arise over time that impede the growth of such enabling technology. The thermal problem is still a serious example of NoC design complications that can greatly limit NoC designs. This forces designers to model, design, and innovate new tools and techniques either offline or at runtime to measure, manage, and solve thermal problems. As a sequel, various techniques have been introduced, covering all layers from the top-most networking application layer to the bottom most-physical layer. In this survey paper, the authors put their hands on various designs and modeling techniques for thermal-aware NoC management. Most importantly, key ideas and research directions are classified, pointed out, and demonstrated with a reasonable amount of details that enables interested researchers to come up and grasp all research directions for thermal-aware NoC technologies.

Index Terms—Thermal Management, Network-on-Chip, System-on-Chip, Manycore Processors, 3D Integration.

1 Introduction

THERMAL problem is one of the most serious challenges in nanotechnologies due to high power density and the growing vulnerability of the temperature effects in delay, leakage, and reliability. NoCs promise to alleviate many of the scaling problems that appear with increasing levels of system-on-chip integration. However, as technology develops, the effects of temperature become more severe from the performance and the reliability perspectives. The designers need to understand the impact of temperature on these systems to reduce thermal hotspots and maintain the specified performance. Thermal hotspots can lead to significant timing issues, forcing designers to opt for wider timing margins that degrade performance. In [1] the authors investigate the impact of high temperatures on link delay and power consumption for different technologies. High temperature effects are observable for all the tested technologies. For example, an operating temperature of 150 °C and a temperature difference of up to 50 °C cause more delay and power overhead in 45 nm and 32 nm technologies, by as much as 71%.

Thermal problems are not only degrading the performance metrics but also chip reliability. Circuit reliability depends exponentially on the operating temperature, where temperature hotspots accounting for most electronic failures [2]. In more details, high temperature profiles can degrade the Mean-Time-To-Failure (MTTF) significantly [3]. This effect on reliability is studied by Sharam et al. in [3]. The authors studied four different lifetime metrics: Thermal Cycles (TC), Stress Migration (SM), Time Dependent Dielectric Breakdown (TDDB), and Negative Bias Temperature Instability (NBTI). As shown in [3] all those metrics are temperature dependent. Consequently, the authors found a strong influence of temperature on the MTTF in NoCs. They found that increasing the topology size which means the increasing traffic density at the central nodes increases the temperature of the hotspot nodes and hence decreases the MTTF. Also, they found a strong inverse relation between the operating clock frequency and MTTF, even between the MTTF and the router buffer size.

Various 3D technologies are affected by temperature variations, photonic or optical Network-on-Chips (OpNoCs) are important examples in that regard. The rise in temperature causes performance degradation of OpNoC components like Laser sources, Micro Ring Resonator (MRR), and optical transceivers. According to [4], the resonant wavelength of MRR shifts approximately linearly with increasing temperatures. For an MRR working at temperature T, the shifted resonance wavelength λ is given by

$$\lambda = \lambda_B + \rho \times (T - T_B) \quad (1)$$

Where, λ_B is the MRR resonance wavelength at the base temperature T_B, and ρ is the shift coefficient in the wavelength of the MRR and it is also a temperature dependent. In addition, the temperature fluctuation in OpNoCs is either resulting in optical signal power loss (increases MRRs losses) or even a complete corruption of data [5]. Therefore, thermal management is indeed of crucial importance when designing NoCs in various technologies.

In this survey, we reviewed different thermal-aware techniques proposed in the literature. The goal is to provide the reader with the techniques, ideas, tools, models, and the state-of-the-art directions in that field of research. To make the survey comprehensive and self-contained we reviewed solutions that belong to different layers, i.e. physical layer, network layer, etc. and also cross-layered ones. Also, and most importantly, we put our hands on the shortcomings in each field of research and propose future research directions that patch those shortcomings. Table 1 shows the most cited or recent surveys [6–15] on NoC field. As shown in the table, most surveys [7–9, 11–13] are focused on the communication infrastructure and paradigm, such as, network topology, router architecture, buffer optimization, routing algorithms, switching schemes, congestion control, energy sufficient, fault tolerance and reliability. Others [6, 10, 14, 15] focus on design, evaluation, implementation and new-technologies. Although thermal problem is one of the most serious issues, thermal management techniques have not been surveyed well. To the best of our knowledge, this survey is the only one on NoC thermal management approaches.

In this survey, the authors review the state-of-the-art techniques for NoC thermal management. First, the authors highlight thermal modeling and sensing in Section 2. After that, thermal sensing and modeling tools introduced so far in literature are

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