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# Photoemission study of interfacial reactions during annealing of ultrathin yttrium on $SiO_2$/Si(1 0 0)

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**Abstract**

X-ray photoelectron spectroscopy (XPS), ultraviolet photoelectron spectroscopy (UPS) and work-function measurements have been used to investigate the Y/$SiO_2$/Si(1 0 0) interfaces in situ as a function of annealing temperature. The results show that yttrium is very reactive with $SiO_2$ and can react with $SiO_2$ to form Y silicate and $Y_2O_3$ even at room temperature. Annealing leads to the continual growth of the Y silicate. Two distinctive reaction mechanisms are suggested for the annealing processes below and above 600 K. The reaction between metallic yttrium and $SiO_2$ dominates the annealing processes below 600 K, while at annealing temperatures above 600 K, a reaction between the new-formed $Y_2O_3$ and $SiO_2$ becomes dominant. No Y silicide is formed during Y deposition and subsequent annealing processes. UPS valence-band spectra indicate the silicate layer is formed at the top surface. After 1050 K annealing, a Y-silicate/$SiO_2$/Si structure free of $Y_2O_3$ is finally formed.


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## 1. Introduction

In recent years, high dielectric constant (high-*k*) metal oxides and silicates have been widely investigated as potential replacements for $SiO_2$ as the gate dielectric material in future complementary metal–oxide–semiconductor (CMOS) devices [1]. Besides a suitable dielectric constant, a $SiO_2$-like high quality interface with silicon is needed for a successful gate dielectric [1,2]. However, most of the reported high-*k* materials present higher midgap interface state densities ($\sim 10^{11}$ to $10^{12}\,cm^{-2}$) with Si than $SiO_2$ ($\sim 2 \times 10^{10}\,cm^{-2}$) [1,2]. It is therefore preferred to have several monolayers of $SiO_2$ serving as a low-defect-density buffer layer between the high-*k* dielectric film and the silicon substrate [2].

There have been many previous studies on the interactions between $SiO_2$ thin layers and metal overlayers [3–6]. The purpose of early studies is to find suitable gate materials in the MOS structures [3,4]. The recent work of Lee et al. suggests that studies on metal/$SiO_2$ interactions are also very helpful for understanding the interface formation at the initial stage of the high-*k* film deposition [5,6]. $Y_2O_3$ and

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yttrium silicate are attractive high-$k$ candidates because of their moderately high dielectric constants, high conduction band offsets and thermodynamically stability on silicon [7–10]. In this work, we investigated the $Y/SiO_2/Si$ interfaces as a function of annealing temperature under ultrahigh vacuum (UHV). The interfacial reactions were monitored in situ at different annealing temperatures by using X-ray photoelectron spectroscopy (XPS), ultraviolet photoelectron spectroscopy (UPS) and work-function measurements. It is found that the Y overlayer can react with $SiO_2$ at room temperature, forming Y silicate and $Y_2O_3$. Annealing leads to the continual growth of the silicate. At temperatures above 600 K, the amount of $Y_2O_3$ decreases with annealing temperature. A Y-silicate/$SiO_2$/Si structure free of $Y_2O_3$ is finally formed after 1050 K annealing.

## 2. Experimental details

The experiments were carried out in an ESCALAB MK II system with a base pressure of $2 \times 10^{-10}$ mbar. The n-type Si(1 0 0) substrate covered by a native $SiO_2$ layer was annealed at 1100 K for several cycles by using resistive heating to remove the contaminants. The surface cleanliness was assessed by the disappearance of the C 1s core-level emission. The yttrium film was deposited onto the oxide surface at room temperature by evaporating yttrium from a well-outgassed tungsten basket. Without leaving the UHV, the sample was transferred into the analysis chamber, where it was subsequently annealed and in situ analyzed at increasing annealing temperature. The annealing temperature was estimated by the heating current according to a current–temperature calibration curve and the annealing time at each temperature was 15 min. UPS spectra were taken using a He I line ($h\nu = 21.2$ eV), and a Mg Kα radiation source ($h\nu = 1253.6$ eV) was used in XPS measurements. Photoelectrons were collected at an emission angle of 15° with respect to the surface normal. The analyzer is in the constant resolution mode, at a pass energy of 5 eV for UPS and 20 eV for XPS. Absolute values of the work function were calculated from the width of the UPS curves (samples bias = −5 V), with an accuracy of ±0.1 eV.

## 3. Results and discussion

Figs. 1 and 2 illustrate the spectral evolution of the Si 2p and O 1s core levels after Y deposition and subsequent annealing at different temperatures, respectively. Both the Si 2p and O 1s spectra were normalized with same height to show the variations of the line shapes. The Si 2p spectrum of the clean $SiO_2$/Si surface can be fitted by four features with binding energies of 99.8, 100.7, 102.0 and 104.1 eV (shown at the bottom of Fig. 1). The main peak at 99.8 eV is due to the underlying Si substrate and the feature at 104.1 eV is typical of $SiO_2$. The other two small features can be attributed to $Si^{1+}$ and $Si^{2+}$ arising from the $SiO_2$/Si interface. The energy separation of 4.3 eV between metallic Si 2p and $Si^{4+}$ 2p is consistent with the reported value [2]. The area ratio between the Si 2p core levels of $Si^0$ and $SiO_2$ is 2.9, which can be used to estimate the thickness of the $SiO_2$ overlayer [11]. The oxide thickness was estimated to be about 16 Å, by assuming that the

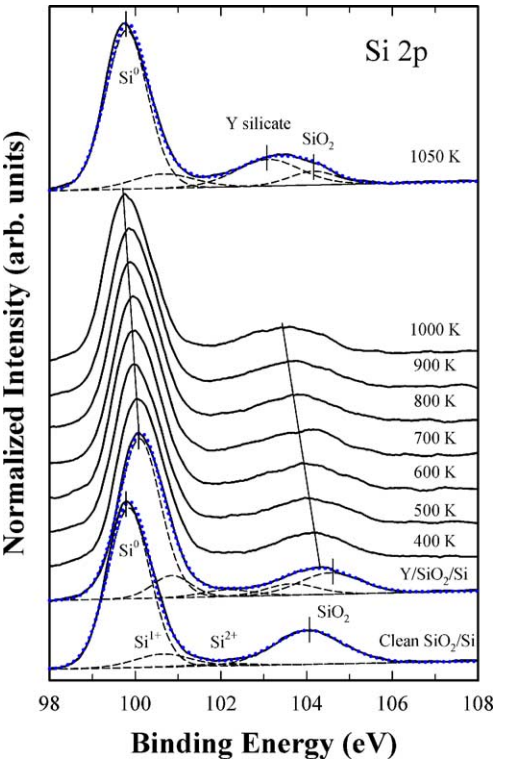


Fig. 1. Si 2p core-level photoelectron spectra obtained from the clean, Y-covered and subsequently annealed $SiO_2$/Si(1 0 0) surface.