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New physical techniques for IC functional analysis of on-chip devices and interconnects

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Abstract

Localization of functional fails in ICs makes use of physical interactions that the devices produce under electrical operation. The focus is on electroluminescence (keyword: photon emission) and signal responses to stimulation by scanned beams of laser light or particles. In modern chip technologies access of this information is only available through chip backside. This paradigm shift requires a full revision of chip analysis techniques and processes. This has also been a kick-off of a rush in development of new methodologies. Here, an overview is given which parameters are crucial for successful analysis techniques of the future and how photon emission, laser based techniques and new preparation techniques based on focused ion beam (FIB) open the path into this direction.

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1. Introduction

The physical techniques for functional analysis of ICs that have been developed along IC technology innovation in the past have been derived from microscopy type interactions. This way, all kinds of image contrasts produced by optical or particle beams could be used to interact with the voltage or current in the IC. This set of methodologies accessed the information through the structured frontside of the planar technology after local decapsulation, and used the imaging power of the respective beams in superposition to locate the physical interactions. Now, with new packaging technologies like flip chip (Fig. 1), local decapsulation can only access the bulk silicon of the chip back side. For the analysis techniques this means a complete paradigm shift [1]. Only signals that are able to pass bulk silicon apply in new chip generations. With moderate thickness of the die, this reduces the options to optical information with photon energies lower than Si band gap, i.e. near IR light (Fig. 2). The next section will introduce the set of techniques that have been developed

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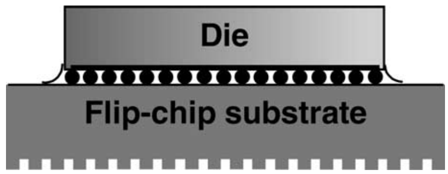

Fig. 1. Flip chip package. Structured side of IC (die) is turned to substrate.

and can be expected in this regime. Recent progresses of focused ion beam (FIB) preparations have opened the path to less than 1 μm local silicon. The options that this breakthrough offers are presented in Section 3.

2. Functional analysis techniques through moderate silicon thickness (50–100 μm)

Global polishing works for moderate 50–100 μm bulk silicon. The preferred analysis techniques in this case are near IR photon emission and laser stimulation.

2.1. Photon emission

Photon Emission (PEM), presented 1986 [3], has become the most effective functional analysis technique in microelectronics in the early nineties (reviews: [4,5]). The technique uses faint light that is emitted by the IC under normal operating conditions, based on radiative relaxation of mobile charge carriers in silicon accelerated in electric field, and/or radiant

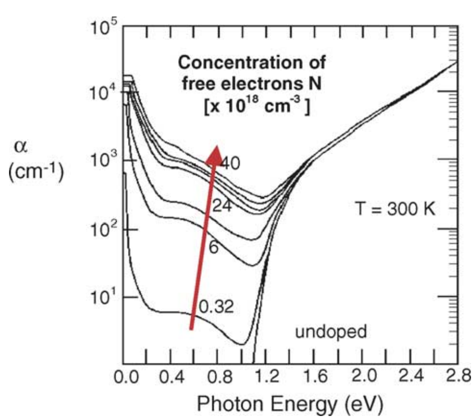

Fig. 2. Spectral absorption in silicon [2].

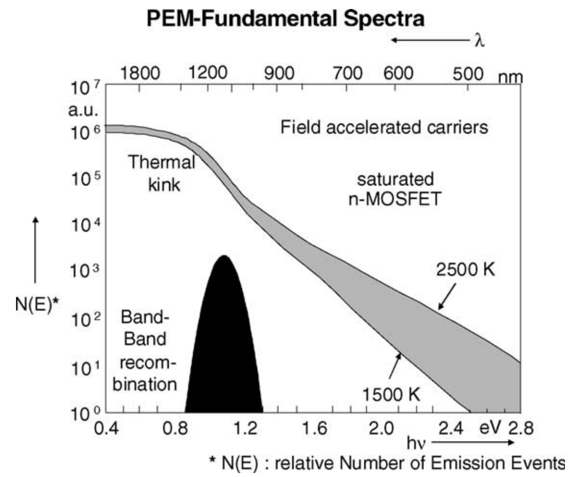

Fig. 3. Photon emission: spectral distribution of FET in saturation.

recombination (spectral distributions: Fig. 3). In static digital CMOS, only failing devices would emit light. This gives PEM a ubiquitous range of uses and is leading for failure localization of static or power down status in ICs. One reason is the relative inexpensive equipment: a silicon CCD can be used as detector. But

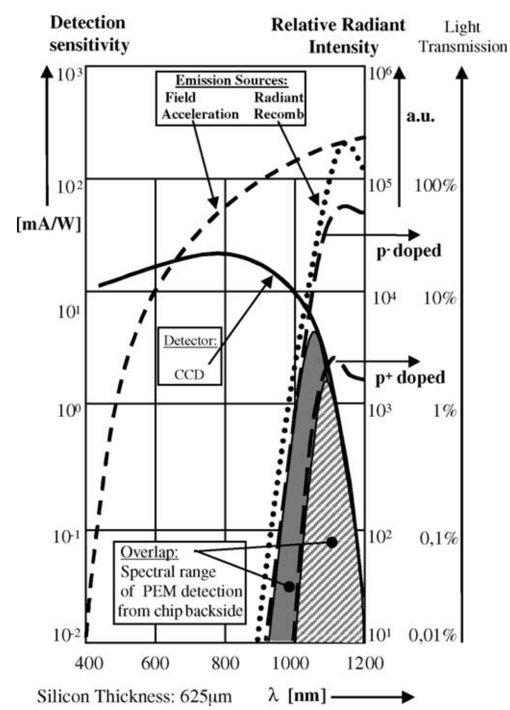

Fig. 4. Spectral response of Si CCD detector and transmission of bulk silicon.