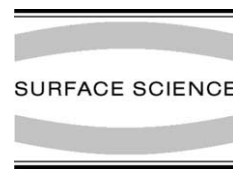




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Surface Science 575 (2005) L51–L56



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Surface Science Letters

Influence of Si deposition on the electromigration induced step bunching instability on Si(1 1 1)

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Received 3 September 2004; accepted for publication 5 November 2004

Available online 28 November 2004

Abstract

Effects of Si deposition on electromigration induced step bunching on the Si(1 1 1)-(1 × 1) surface were studied for “temperature Regimes” I (~850–950 °C) and II (~1040–1190 °C) on “dimpled samples” that have a range of initial surface miscut angles ($\pm 0.5^\circ$). We find that a step-down electric current is required to induce bunching under both net sublimation and depositions conditions in temperature Regime I, in agreement with previous reports. However, for temperature “Regime II” we observe that step-up current is required to induce step bunching for *both* net deposition and net sublimation conditions, in contradiction with the report of Métois and Stoyanov [Surf. Sci. 440 (1999) 407] and suggested “step permeability” model of Stoyanov [Surf. Sci. 416 (1998) 200]. We further observe a strong reduction in the number of crossing steps on the wide terraces for near equilibrium Si flux conditions. We also report a systematic, nearly linear dependence of the step bunching rate on the initial sample miscut angle in both Regimes I and II, which is independent of net deposition/sublimation conditions.

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Keywords: Atomic force microscopy; Diffusion and migration; Evaporation and sublimation; Growth; Step formation and bunching; Surface diffusion; Surface structure, morphology, roughness, and topography

1. Introduction

Understanding the processes that govern the motion of vicinal surface steps has been a long-standing problem of great fundamental interest in surface science. For semiconductors, understanding the behavior of surface steps is technologically critical for the growth of epitaxial overlayers

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and for device processing. Recently there has been great interest in processes that lead to spontaneous rearrangement of steps into surface structures of size ranging from a few nm up to many μm [1–5].

Since 1988 [6] it has been known that heating a slightly-miscut Si(111) with direct current (DC) in an ultra-high vacuum (UHV) environment leads to large scale changes in surface morphology such as the formation of step bunches. The earliest reports of these “surface electromigration” phenomena by Latyshev and coworkers [6] showed that step bunching on Si(111) only results for one direction of the current relative to the vicinal “step-up” or step-down” direction (see Fig. 1(a)), but also that this required current direction reverses multiple times with increasing temperature. In temperature “Regime I” ($\sim 850\text{--}950\text{ }^\circ\text{C}$) and “Regime III” ($\sim 1200\text{--}1300\text{ }^\circ\text{C}$) bunching occurs only for step-down heating current, while in “Regime II” ($\sim 1040\text{--}1190\text{ }^\circ\text{C}$) and “Regime IV” ($>1320\text{ }^\circ\text{C}$) bunching occurs only for step-up heating current. In all temperature regimes the opposite current direction maintains an initially-vicinal surface and accelerates relaxation of an initially step-bunched surface [7].¹

Still controversial is the physical origin of these temperature-dependent reversals of the current direction required for step bunching. It is generally accepted that the diffusing surface species (thought to be individual Si adatoms for Si(111)) each have an effective charge q_{eff} that causes them to drift (or flow) either parallel (for $q_{\text{eff}} > 0$) or antiparallel (for $q_{\text{eff}} < 0$) to the applied electric field. It is also generally agreed that a step-down adatom flow will cause a bunching instability provided steps have a sufficiently small attachment probability and are sufficiently “impermeable” (i.e., a diffusing surface atom must incorporate into a step before it can cross onto the adjacent terrace [8]). One general model proposed that q_{eff} changes sign as the temperature is increased so that adatom flow is parallel to the applied electric current in Regime

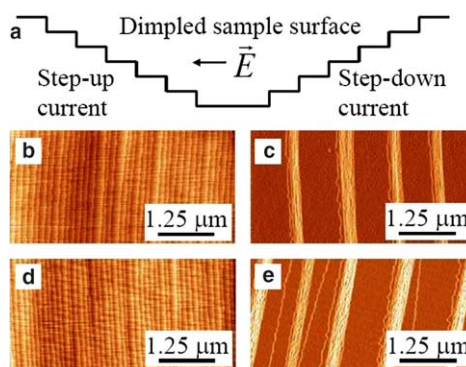


Fig. 1. (a) Schematic view of vicinal stepped surface close to the bottom of a spherical dimple. For right-to-left applied electric field (and conventional current) direction, the left side (right side) has step-up (step-down) current. (b) and (c): derivative-mode AFM images (which appear as if illuminated from the left) of the surface annealed for 3.0 h at $940\text{ }^\circ\text{C}$ under free sublimation conditions ($R_{\text{net}} \cong -0.002\text{ } \text{\AA}/\text{s}$) for (b) step-up and (c) step-down current. (d) and (e): surfaces annealed at $940\text{ }^\circ\text{C}$ under net deposition of $0.01\text{ } \text{\AA}/\text{s}$ for (d) step-up and (e) step-down current conditions. Bunching is only seen for step-down current for both net-sublimation and net-deposition conditions.

I and Regime III, and anti-parallel in Regime II and Regime IV [9,10]. In this case there will be step-down adatom flow (and hence bunching) only for step-down (step-up) electric current in Regimes I and III (Regimes II and IV). Another general view is that adatom flow is always parallel to the applied electric field (i.e., q_{eff} is always positive) but that temperature-dependent changes to the step permeability [11,12] or to the relative adatom diffusivity close to a step edge [13] lead to bunching even for step-up adatom flow. Here we focus on the model proposed by Stoyanov [11] and supporting experimental evidence [12] which hold that significantly increased step permeability in Regime II causes step bunching for a step-up adatom flow in that regime. A key prediction of this model is that permeable steps will bunch for step-up adatom flow *only* under “net sublimation” conditions (when the Si sublimation rate R_{sub} is larger than an applied Si deposition rate R_{dep}) while a step-down flow is required to produce bunching under “net deposition” conditions ($R_{\text{sub}} < R_{\text{dep}}$). Métois et al. [12] reported observations that bunching in Regime II indeed follows this predicted pattern, with step-up current required for bunching under

¹ As addressed later, so called “in-phase step wandering” has sometimes been observed for step-down current in regime II.

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