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Reliability evaluations of flip chip package under thermal shock test

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Abstract

The microstructural investigation and thermo-mechanical reliability evaluation of the Sn–37Pb solder bumped flip chip package were carried out during the thermal shock test of the package. In the initial reaction, the reaction product between the solder and Cu mini bump of the chip side was Cu_6Sn_5 IMC layer, while a layer of Ni_3Sn_4 was formed between the solder and electroless Ni–P layer of the package side. The primary failure mechanism of the solder joints in this type of test method and package was confirmed to be thermally activated solder fatigue failure. The brittle interfacial failure mode was sometimes detected from the cross-sectional studies, but nearly whole of the failed packages showed the occurrence of the typical fatigue cracks. The finite element analyses were conducted to interpret the failure mechanisms of the packages. The finite element analyses revealed that the cracks were induced by the accumulation of the plastic work.

Keywords: Flip chip; Thermal shock test; Thermal fatigue; Solder; Sn-37Pb

1. Introduction

The performance and function of electrical devices have increased drastically in the area of network servers and switches [1–3]. In the field of leading-edge devices, the flip chip package is recognized as one of the most effective packages for high pin count and high electrical performance. The flip chip interconnection is the connection of an IC chip to a carrier or substrate with the active face of the chip facing toward the substrate. The flip chip technology is generally considered the ultimate first level connection because the highest density can be achieved and the path length is shortest so that optimal electrical characteristics are achieved.

Thermally activated solder fatigue and a premature brittle interfacial fracture at the intermetallic compound (IMC) layers are the major wear-out

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failure modes in the flip chip packages, caused mainly by mismatch in thermal expansion coefficients between the silicon die and substrate [4]. The fatigue failures occur as a result of the damage in the solders produced by the cyclic inelastic strains [5–7]. On the other hand, the brittle nature of the IMC layers between the solder and under bump metallization is the driving force for the premature brittle interfacial fractures. Previous studies on the flip chip packages have shown that the plastic work and the creep strain play a predominant role on the fatigue life of the flip chip packages, while the formation of the continuous IMC layers is the main cause for deterioration of the solder joint reliability [8,9]. However, these results are mostly obtained from the computational simulations such as finite element modeling, and there are very limited researches concerning the microstructural behaviors in the solder joints. The experimental investigation as well as the computational simulation is essential for the evaluation of the failure mechanism.

Therefore, we focused the investigations of the failure behaviors in the solder bumped flip chip packages during reliability testing with both the experimental and finite element analyses. Scanning electron microscopy (SEM) and electron probe micro analyzer (EPMA) were employed to investigate the microstructure and phase analysis of the solder joints. The thermal shock test was chosen for the reliability evaluation of the solder joints, because this test can compress the testing time by $5X$, reducing the qualification time and cost. Then, the cross-sectional study was conducted to investigate the failure behavior of the solder bumps. Finally, the computational simulation employing a finite element modeling (FEM) was conducted to interpret the failure mechanism.

2. Experimental and analysis procedures

The solder composition used in this study was Sn–37Pb (in mass%). The flip chip solder bumps were made by a modified low cost flip chip bumping process employing stencil printing of solder paste and Cu plating without using thick photoresist. The Cu-mini bumps were formed with the electroplating method in the control of current density and plating time. The detailed flip chip solder bumping process could be found in our previous research [10]. After the solder bumps were made on the silicon wafer, the chip was flipped and bonded to bismaleimide triazine (BT) substrate using a flip chip bonder (FINEPLACER-96LAMBDA, Finetech).

The reliability of the flip chip bonded packages was tested by means of the thermal shock in the range 233–398 K (15 min cycle time, air to air, 6 min dwelling time). After the thermal shock test, the specimens were mounted in epoxy, and then the cross-sectional studies were carried out by grinding with SiC papers followed by subsequent polishing with 1 and 0.3 μm alumina powders. The cross-section was conducted through the diagonal line of the package. The microstructural observation was conducted with SEM, and the resulting IMCs were measured by EPMA.

Finite element simulations were performed to determine the stress behaviors within the flip chip package when it is stressed by the temperature cycles from the environment. The finite element code used in this study was ANSYS, release 8.0. Schematics of the 3-dimensional (3-D) finite element model are shown in Fig. 1. Due to the symmetry of the package geometries, only one-eighth of the flip chip assembly was modeled using a 3-D-1/8th finite element analysis symmetry model along the two symmetry planes. The solder joints along the diagonal cross-sectional symmetric plane are shown in Fig. 1(b). As shown in Fig. 1(b) and (c), the full details of the actual packages such as sputtered Ti/Cu layer and thin SiO_2 passivation layer were implemented in the model to catch the highest degree of the accuracy. The 3-D VISCO107 and SOLID185 elements were employed to model the solder and the other components containing Si chip and SiO_2 layer, etc., respectively. Because the thermal shock test temperature was in excess of a homologous temperature of 0.5, linear and non-linear, time-dependent and independent material properties were incorporated in the finite element model. In the present work, the Anand constitutive equations were used to realize the exact deformation