Available online at www.sciencedirect.com
SCIENCE DIRECT®
Microelectronic Engineering 80 (2005) 296–304
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Current status and challenges of ferroelectric memory devices

H. Kohlstedt, Y. Mustafa*, A. Gerber, A. Petraru,
M. Fitsilis, R. Meyer, U. Böttger* and R Waser*

Forschungszentrum Jülich, Institut für Festkörperforschung, IFF and the Center of Nanoelectronics for Informationtechnology CNI, Germany
**Institut für Werkstoffe der Elektrotechnik, RWTH Aachen 52056 Aachen, Germany*
Tel: +49-(0)24616161-2994 email: h.h.Kohlstedt@fz-juelich.de

Abstract

We report on the state-of-the art memory devices on the basis of ferroelectric materials. The paper starts with a short survey on competitive non-volatile memory technologies and focuses then on ferroelectric memories. This includes the ferroelectric random access memory (FeRAM) and the ferroelectric field effect transistor (FeFET). Cell layouts, material aspects and CMOS compatibility as well as fabrication issues will be discussed.

Beside the current research on ferroelectric memory devices we present results on the superparaelectric limit of ferroelectric materials with respect to lateral and thickness scaling. Scanning probe techniques showed ferroelectric properties in dots as small as 20 nm. Ultra thin ferroelectric films as thin as a few unit cells can be achieved on lattice matched substrates. These investigations can be considered as a guideline for the maximum achievable packaging density of FeRAMs including low power consumption. The most challenging task to achieve storage above 128 Mb, is the conformal coverage of 3-D electrodes, e.g. by atomic layer deposition (ALD). Three dimensional capacitors are mandatory to achieve sufficient charge for clear signal sensing.

In addition, we present a few new concepts based on ferroresistive films, strain induced enhanced ferroelectricity, and lead-free ferroelectrics which may be relevant for the future FeRAM technology. Finally, a new challenging concept of an entire organic ferroelectric field effect transistor (OFeFET) is briefly discussed.

Keywords: Nonvolatile memories; FeRAM; ferroelectrics; conformal coverage, scaling

1. Introduction

There are worldwide considerable efforts to develop nonvolatile random access memories. Portable electronic equipment such as the personal digital assistant, cellular phones or digital cameras need secure and fast data transfer in combination with nonvolatile storage. Another main development route is that of contact less smart cards with multiple functions including e.g. personal banking, transport access and medical data.

The market for non-volatile random access memories (NVRAMs) has been drastically increased over the last years, although by far not reaching the market volume of (volatile) dynamic random access memories (DRAMs). The required performance of NVRAMs, such as, storage density, endurance, write

0167-9317/$ - see front matter © 2005 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2005.04.084

and access time or power consumption are related to a particular application. Therefore it is not astonishing that a number of different NVRAMs technologies exist to fulfill all requirements. In a short survey we will summarize today's most promising NVRAM technologies [1]. Then the paper focuses on ferroelectric random access memories (FeRAMs) and ferroelectric field effect transistors (FeFETs) highlighting the following issues: scaling, material aspects including CMOS (complementary metal oxide semiconductor) compatibility and electronic properties. In the last section we describe challenging tasks as 3-dimensional (3-D) conformal coverage of complex oxides, lead free ferroelectrics and strain induced enhancement of the spontaneous polarization P_s. Although a bit beyond of the scope of this paper, we will shortly mention the work on ferroelectric polymers including an entire polymer FeFET.

2. NVRAMs – a short survey

In general we can distinguish between charged based and resistive based NVRAMs. To make this point clear, we relate this definition to the mechanism of the read operation. If the bit-line (BL) is charged via a resistor, the technology belongs to the class of resistive storage. In case the charge of a capacitor is sensed, the technology is defined as charged based storage. Resistive storage readout is non-destructive, whereas a charge based approach has a destructive readout and the bit has to be reprogrammed after a read cycle.

What are the main competitors among NVRAMs? Well established technologies are Flash and EEPROMs [2]. A Flash memory cell is basically a MOSFET with an additional floating gate. Depending on the charge on the floating gate the threshold voltage of the transistor (1T-cell) is high or low and the cell acts therefore as a non-volatile storage device. The integration capability is even larger than for DRAMs. Large programming times and voltages as well as limited endurance due to high-field programming stress are the most important concerns with Flash. The advent of nano dot floating gates improved drastically the endurance [3]. A new development of so-called crested tunnel barriers (NOVORAM) [4] for the gate oxide will maybe increase the programming speed and also reduce the high-field stress.

Magnetic tunnel junctions (MTJs) are another promising approach. Here the information is stored via spin-dependent tunneling. The computational "0" and "1" are represented by parallel or anti-parallel alignments of the magnetization vectors of the bottom and top electrodes of an MTJ. Although this effect has been discovered already in 1975 by Juliére [5] the breakthrough for industrial applications came in 1995 by using amorphous Al_2O_3 as barrier and Co (or CoFe alloys) as electrodes [6]. Recently the signal amplitude $\Delta R/R$, was increased to about 220% by using MgO as tunnel barrier [7]. Magnetic Random Access Memories (MRAMs) are currently in the pilot line by, e.g., the consortium IBM/Infineon and Freescale. First products with MRAMs will appear this year on the market. Nonetheless, cross talk problems between neighboring cells and the relative high power consumption during programming may result in some limits for applications.

In 1968, Ovshinsky presented a resistive storage device on the background of a phase-change effect [8]. The technology is called either Ovonic or (phase change) PCRAM. The principle idea is that the resistance of chalcogenics depends whether the material is in the amorphous or in the crystalline state. Programming is achieved by a particular data sequence. Ovonics are developed for example by Intel and ST Microelectronics.

Since the 60`s of the last century research efforts focused on resistive switching in binary oxides as Nb_xO_y, Al_2O_3, Ta_xO_y, etc. in metal-insulator-metal configurations [9]. Nowadays, a number of new materials, ranging from polymers to complex oxides, have been successfully applied as resistive storage elements and are attracting much interest. Nonetheless, the lack of a deeper understanding of the underlying physical and chemical processes and the insufficient reliability ask for more research before these candidates can play a serious role in NVRAM technology.

FeRAMs (a charged based device) and FeFETs (a resistive based device) make use of the (two) switchable remnant polarization states of ferroelectric materials by an external electric field. FeRAMs one can find today in applications as game stations or the RF tag with moderate storage densities of 256 MB.

Download English Version:

https://daneshyari.com/en/article/9670512

Download Persian Version:

https://daneshyari.com/article/9670512

Daneshyari.com