

Use of ferroelectric gate insulator for thin film transistors with ITO channel

E. Tokumitsu, M. Senoo, T. Miyasako

*Precision and Intelligence Laboratory, Tokyo Institute of Technology
4259-R2-19 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan
Tel: 81-45-924-5084 email: tokumitsu@neuro.pi.titech.ac.jp*

Abstract

Typical n-channel transistor characteristics with nonvolatile memory operation of ferroelectric-gate thin film transistors (TFTs) using indium-tin-oxide (ITO) channel have been demonstrated. It is shown that relatively large “on” current can be obtained in ITO/(Bi,Li)₄Ti₃O₁₂ (BLT) TFTs. Since the calculated field-effect mobility is as small as 4 cm²/Vs, the large “on” current is due to the large charge density induced by the ferroelectric gate insulator. It is also shown that the thin conductive ITO channel can be depleted completely by the ferroelectric polarization and “off” current of the device is as low as 10⁻⁷ A. Drain current - gate voltage characteristics exhibit counterclockwise hysteresis due to the ferroelectric nature of the gate insulator, which demonstrates nonvolatile memory operation. The memory window is approximately 4 V, which agrees with the theoretical calculation. In addition, no change in both “on” and “off” currents has been observed up to 10³ s.

Keywords: ferroelectric film, ferroelectric-gate transistor, nonvolatile memory, thin film transistor, ITO, (Bi,Li)₄Ti₃O₁₂

1. Introduction

Use of a ferroelectric thin film as a gate insulator for conductivity control of the semiconductor channel in the field-effect transistor (FET) was proposed as early as 1960 [1,2]. Such ferroelectric-gate transistors exhibit nonvolatile memory operation because of the remanent polarization of the ferroelectric gate insulator. However, ferroelectric-gate transistors are still in the laboratory development stage and usually suffer from short data retention time.

There are mainly two difficulties in the Si-based ferroelectric-gate transistors. First is the difficulty to fabricate good interface between the ferroelectric layer and the silicon substrate. It is well known that the ferroelectric films need high temperature annealing in oxygen ambient to be crystallized and that such a process produces an interfacial layer between the ferroelectric film and the Si with poor electrical properties. Hence, a buffer layer is usually inserted and metal-ferroelectric-insulator-semiconductor (MFIS) structure has been used to

fabricate ferroelectric-gate transistors. [3-5] Second difficulty is “charge-mismatch” problem. The remanent polarizations of most ferroelectric materials are 10-30 $\mu\text{C}/\text{cm}^2$, while the charge amount required to control the channel conductivity of MOSFET is usually around or less than 1 $\mu\text{C}/\text{cm}^2$. Even if the breakdown field of 10 MV/cm is applied to the SiO_2 gate insulator, the induced charge is only 3.5 $\mu\text{C}/\text{cm}^2$. Hence, only small part of the ferroelectric polarization can be used in Si-based devices, which is probably one of the reasons for their short data retention time.

In this work, we demonstrate nonvolatile memory operation of a ferroelectric-gate thin film transistor which has an indium-tin-oxide (ITO) as a channel material instead of silicon. Since both the ferroelectric gate insulator and the channel are oxide-based, good interface properties are expected. In addition, even though ITO is a conductive oxide with high carrier concentration, theoretical consideration shows the ITO channel can be depleted if it is sufficiently thin, because the ferroelectric gate insulator can induce much larger charge density than the normal gate insulator such as SiO_2 and HfO_2 . Hence, full polarization of ferroelectric materials can be used in the presented device and long data retention time is expected.

2. Experimental procedure

We have fabricated thin film transistors (TFTs) with bottom gate structure because crystallization temperature for the ferroelectric thin film is higher than that of ITO. Schematic illustration of the fabricated device is shown in Fig.1. First, Pt/Ti (50nm/20nm) was vacuum evaporated on SiO_2/Si substrate and the bottom gates are patterned. Then, ferroelectric $\text{Bi}_{4-x}\text{La}_x\text{Ti}_3\text{O}_{12}$ (BLT) thin film was spin-coated by the conventional sol-gel technique. BLT film was crystallized at 700°C for 30min in O_2 atmosphere. Next, thin ITO film was deposited by RF sputtering using an ITO ceramic (10wt% SnO_2) target in Ar/O_2 atmosphere. Next, Pt source and drain electrodes were vacuum evaporated and patterned. Finally, the device region was isolated by the reactive ion etching (RIE). The thicknesses of the BLT gate insulator and the ITO channel are 200-210 and 10 nm, respectively. The channel length (L)

of the fabricated devices is varied from 40 to 120 μm with a constant channel width (W) of 120 μm .

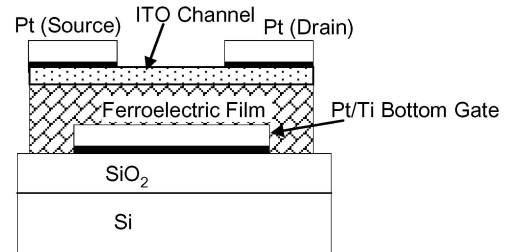


Fig.1 Schematic illustration of ferroelectric-gate TFT with bottom gate structure fabricated in this work.

3. Results and discussion

Fig.2 shows the measured drain current - drain voltage (I_D - V_D) characteristics of fabricated ferroelectric-gate TFT with a channel length, L, of (a) 120 and (b) 40 μm . The device shows typical n-channel transistor characteristics and exhibits clear current saturation. Note that relatively large “on” currents of 0.43 and 0.97 mA were obtained for the devices with $L=120$ and 40 μm , respectively, when $V_G=V_D=8\text{V}$.

We can estimate field-effect mobility μ by assuming that the saturated drain current is given by the following equation as in the MOSFETs,

$$I_{DS} = \frac{C_i \mu W}{2L} (V_G - V_T)^2 \quad (1)$$

where C_i is the capacitance per unit area of the gate insulator and equivalently given by $P(V_G)/V_G$. $P(V_G)$ is ferroelectric polarization as a function of gate voltage and estimated approximately 20 $\mu\text{C}/\text{cm}^2$ when $V_G=8\text{V}$ from the polarization-voltage (P-V) hysteresis loop of the BLT film. Using this value and a threshold voltage of -1V, we estimate the field-effect mobility to be 4.3 and 3.2 cm^2/Vs for the devices with $L=120$ and 40 μm , respectively. These values are comparable with the reported mobilities for the TFT devices with polycrystalline conductive oxide channels [6-9].

The “on” current at $V_D=V_G=8\text{V}$ is plotted in Fig.3 as a function of the reciprocal of gate length (L). It is found that the “on” current is proportionally increased with $1/L$. An “on” current of about 1 mA was obtained for the device with channel length of 40

Download English Version:

<https://daneshyari.com/en/article/9670513>

Download Persian Version:

<https://daneshyari.com/article/9670513>

[Daneshyari.com](https://daneshyari.com)