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Electron mobility in multi-FinFET with a (111) channel surface fabricated by orientation-dependent wet etching

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Abstract

This paper presents, for the first time, the experimental electron mobility in FinFETs with a (111) channel surface fabricated by the orientation-dependent wet etching. The maximum electron mobility (u_{eff}) is around 300-cm^2/V-s, which is close to that in the (111) bulk MOSFETs. Moreover, the value of u_{eff} is comparable or better than the reported ones in the usual FinFETs with a (110) channel surface prepared with careful surface treatments. This result indicates that the quality and channel surface roughness of the Si-fins by the orientation-dependent wet etching are much better than those fabricated by the conventional reactive ion etching (RIE) process.

Keywords: FinFET; Double-gate MOSFET; Orientation-dependent wet etching; Rectangular cross-section Si-fin; Mobility

1. Introduction

Recently, fin-type double-gate [1] MOSFET (FinFET) [2] has widely been investigated due to its excellent short-channel effects (SCEs) immunity and its simple fabrication processes. However, electron mobility in the usual FinFETs with a (110) channel surface is much smaller than that in (110) bulk MOSFETs because serious plasma damage is introduced on the channel surface during the Si-fin fabrication by reactive ion etching (RIE) [3, 4]. To remove the surface damage, sacrificial oxidation and hydrogen annealing should be forced. Moreover, the sidewall roughness also results in electron mobility

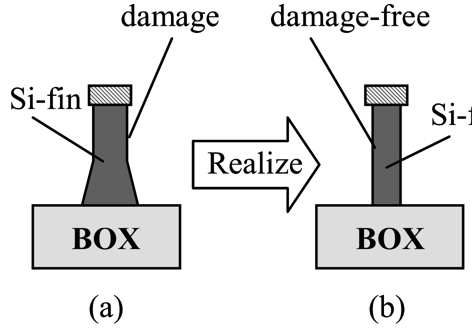

Fig. 1. Comparison between (a) bell-shaped Si-fin by RIE and (b) the proposed ideal rectangular cross-section Si-fin by the orientation-dependent wet etching

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degradation [3]. On the other hand, recently, damage-free ideal rectangular cross-section Si-fin channels with a (111) plane have been developed by orientation-dependent wet etching [5-9]. However, there have been no reports regarding the electron mobility in FinFETs with a (111) channel surface.

This paper presents, for the first time, the experimental electron mobility in the multi-FinFET with a (111) channel surface fabricated by the orientation-dependent wet etching.

2. Fabrication process

To improve the Si-fin channel shape and quality in usual FinFETs as shown in Fig. 1(a), we developed orientation-dependent wet etching. We found that the etching rate for a (111) Si wafer is extremely lower than those for other planes as shown in Fig. 2. This indicates that the (111) plane should remain at the early stage of the etching process.

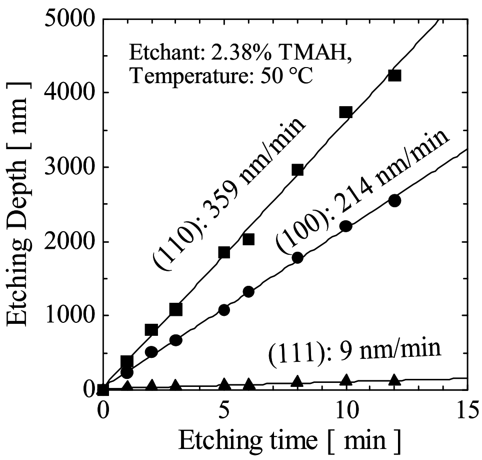

Fig. 2. Etched silicon depth versus etching time in TMAH at 50 °C. The selectivity of (110)/(111) is about 40.

Figure 3 shows the cross-sectional SEM image of the fabricated 16-nm-thick Si-fin channels with (111)-oriented sidewalls. In the multi-FinFET fabrication, we used p-type (110) SOI wafer as a starting material. First, the wafers were thermally oxidized and fin patterns were formed in parallel with <112> direction as shown in the insert in Fig. 3. Then, fin-hard masks were formed by RIE and the SOI was etched by a 2.38% TMAH solution to form upright Si-fin channels. After the Si-fin formation by the wet etching, the gate oxide was directly formed on the (111) sidewalls of the Si-fins without any surface treatment. Subsequently, the n^+ poly-Si gate was formed by EB-lithography and RIE. After PSG deposition, the shallow phosphorus doping for the source-drain (S-D) extension regions was performed by rapid thermal annealing (RTA). Finally, aluminium electrodes were formed and sintered in a forming gas ambient at 450 °C for 30 min.

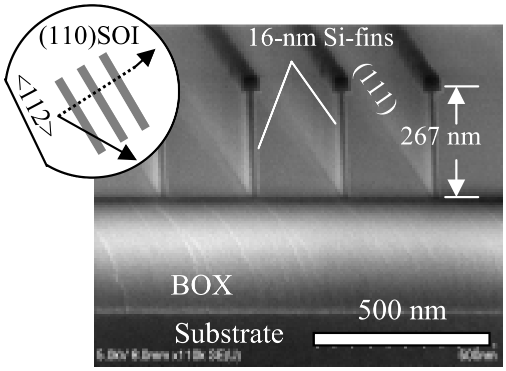

Fig. 3. SEM image of the fabricated 16-nm-thick Si-fin channels. Insert is the schematic fin-patterns on (110) SOI.

3. Results and discussion

The cross-sectional SEM image of the fabricated 5-fin channel device is shown in Fig. 4. It is clear that the Si-fin thicknesses are very uniform and the Si-fin shape shows a perfect rectangular cross-section.

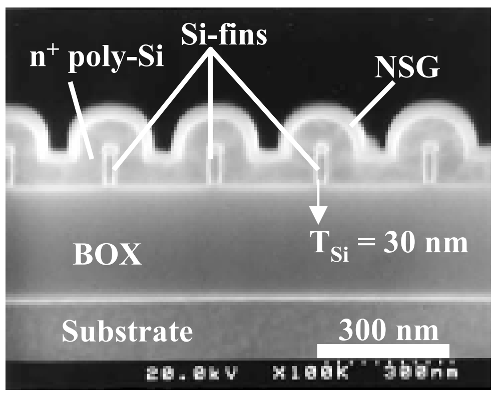

Fig. 4. Cross-sectional SEM image of the fabricated multi-fin channels after gate oxidation, n^+ poly-silicon and NSG deposition. The Si-fin channels show a perfect rectangular cross-section.