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Electron beam lithography for nanometer-scale planar double-gate transistors

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Abstract

Double-gate transistors are promising successors to conventional bulk MOSFETs, since their gate arrangement limits short channel effects yielding better device performance, even at nanometer size gate lengths. An electron beam lithography process for patterning and aligning the nanometer-size gates of a planar double-gate transistor has been constructed. The gates are structured non self-aligned on both sides of a thin c-Si layer, whereby the first structured gate layer together with the c-Si layer is transferred to a handling wafer using wafer bonding and wafer back-side etching, enabling access to the backside of the c-Si layer. Top and bottom gates have been aligned with 25 nm accuracy using topographic marks that are detectable in both exposure steps. Gate lengths of less than 20 nm were structured using the hydrogen–silesquioxane (HSQ) resist. With the help of Monte Carlo simulations the optimal electron acceleration voltage was determined to obtain the best resolution possible when patterning top and bottom gates. An intra-proximity correction was introduced for the acceleration voltage used by varying the dose factor of every pattern to be written.
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Keywords: Double-gate MOSFET; Electron beam lithography; HSQ; Calixarene; Layer transfer; Wafer bonding

1. Introduction and process flow

Multi-gate transistor concepts have been evaluated as promising successors to conventional bulk metal oxide field effect transistors (MOSFETs) for future nanometer scaled miniaturization, since their geometry arrangement effectively reduces the penetration of lateral electric fields into the channel region, thereby minimizing short channel effects [1]. The planar double-gate transistor (PDGT), seen in Fig. 1 is a fabrication variant of multi-gate transistors. This concept utilizes the original surfaces of the top silicon layer of a silicon on insulator (SOI) wafer for the channel regions,

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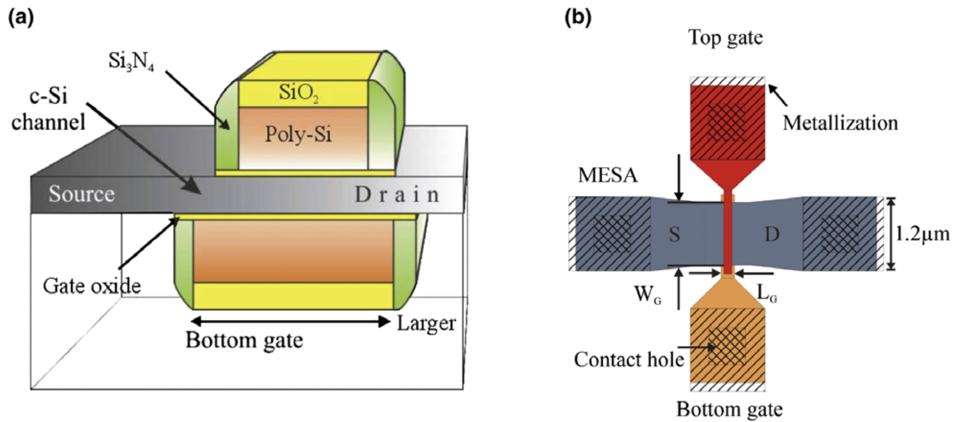

Fig. 1. Planar double-gate transistor. (a) Schematic cross-section view, misaligned gates overlap since the bottom gate is larger. (b) Top design view of the transistor. The cross-section between top and bottom gate and the c-Si MESA defines the channel region. The width of the MESA at the cross-section is the gate width W_G, whereas the geometrical gate length L_G is the gates line width.

which is advantageous due to the smoothness and parallelism of the two surfaces. On the other hand, the device fabrication introduces some technological challenges concerning the patterning of the bottom gate.

The solution implemented here adds wafer bonding into the fabrication sequence as proposed in [2,3]. The process flow can be seen schematically in Fig. 2. After first structuring the bottom gate on a ''donor'' SOI wafer with electron beam lithography (EBL) and anisotropic nano etching (Fig. 2(a)), it is covered with a 300 nm thick TEOS (tetraethylene–oxisilane) oxide which is planarized with chemical mechanical polishing (CMP). The wafer is bonded onto a handling wafer with undensified thermal oxide [4] Fig. 2(b), and turned upside down for further processing, Fig. 2(c). The backside bulk-silicon and buried oxide (BOX) of the donor wafer are etched away, uncovering the bottom surface of the mono-crystalline SOI layer above the bottom gate. The thickness of this Si layer is defined by the SOI material and is, therefore, not dependent on lithographic and etching processes as for the FinFET case [1]. The active region is defined with an optical lithography and MESA etching Fig. 2(d). Subsequently the top gate and the remaining transistor essentials are fabricated as in the conventional SOI transistor process Fig. 2(e). The critical gate alignments are performed by an EBL process with mark detection.

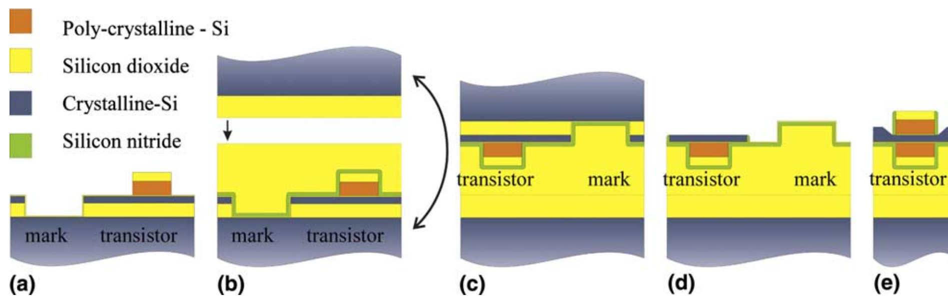

Fig. 2. Fabrication process of the planar double gate transistor. (a) e-Beam mark etching into c-Si and BOX and posterior bottom gate structuring. (b) Silicon nitride and TEOS deposition, bonding of handle wafer on top. (c) The bonded wafers turned upside down for posterior processing. (d) Backside etching of SOI wafer and active region definition. (e) Top gate fabrication and raise of the source/drain regions.

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