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SCIENCE DIRECT®
Microelectronic Engineering 78–79 (2005) 212–217
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Highly selective etch process for silicon-on-insulator nano-devices

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Available online 30 December 2004

Abstract

Reactive ion etch (RIE) processes with HBr/O_2 chemistry are optimized for processing of functional nanostructures based on silicon and polysilicon. The etch rate, etch selectivity, anisotropy and sidewall roughness are investigated for specific applications. The potential of this process technology for nanoscale functional devices is demonstrated by MOSFETs with 12 nm gate length and optimized photonic devices with ultrahigh Q-factors.

Keywords: HBr; ICP-RIE; SOI; EJ-MOSFET; Microring resonator; Silicon photonics

1. Introduction

The International Technology Roadmap for Semiconductors (ITRS) predicts the necessity of novel, non-planar metal-oxide-semiconductor field effect transistors (MOSFETs) to fulfill its stringent scaling guidelines [1]. Candidates for such three-dimensional devices are transistors with multiple gates such as FinFETs or Triple-Gate MOSFETs, usually fabricated on silicon-on-insulator (SOI) substrates [2–5]. SOI technology for multi-gate CMOS, however, results in a three-dimensional topography and therefore imposes new challenges for reactive ion etch (RIE) processes. In detail, an extremely high etch selectivity of polysilicon gates over thin gate oxides has to be achieved while maintaining anisotropic profiles [6–9].

In addition, SOI material enables high integration density for photonic devices due to the large

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doi:10.1016/j.mee.2004.12.029

contrast in refractive index of silicon and silicon dioxide (SiO_2). For low-loss SOI photonic solutions, it is critical to optimize manufacturing tolerances and especially to minimize surface roughness of etched sidewalls [10].

In the first part of this work an inductively coupled plasma reactive ion etch (ICP-RIE) process is described, which meets the requirements concerning high etch selectivity, anisotropy and smooth surface morphology for device fabrication on SOI substrates. In the second part two applications are described. First, electrical characteristics of 12 nm electrical junction (EJ-MOSFETs) are presented. These devices are excellent test structures to prove the limits of scalability down to the deca-nanometer regime [11,12]. Second, high quality microring resonators are shown to demonstrate the low losses of optical wave guides fabricated with the developed etch technology.

2. Experimental

An etch process for structuring silicon and polysilicon with dimensions down to the deca-nanometer regime has been developed using an Oxford Instruments Plasmalab System 100 ICP-RIE tool. The ICP source is supplied with RF power at 2 MHz from a 5 kW generator. An aluminum lower electrode is independently biased with 13.56 MHz RF power from a generator with a maximum power of 600 W. The sample temperature has been maintained at 10 °C during etching using backside helium cooling. All experiments have been performed using a three step etch process: first a native oxide breakthrough using Cl_2 as a reactive gas, second a main etch step using a mixture of HBr and Cl_2 and third an overetch step using a mixture of HBr and O_2. Lithography for the applications described in this paper has been carried out with a high resolution Leica EBPG-5000 e-beam system using hydrogensilsesquioxane (HSQ) resist [13,14].

The ICP plasma parameters of the first step are 50 sccm Cl_2 flow and a chamber pressure of 5 mTorr. In the second or main step, anisotropic etching is performed with a mixture of Cl_2 (25 sccm) and HBr (65 sccm) at an RF power of $P_{RF} = 100$ W, an ICP power of $P_{ICP} = 150$ W, and a pressure of 5 mTorr. The parameters for step 1 and step 2 have been kept constant for all experiments. The etching time for the main (second) step is set to stop at a residual thickness of about 10 nm. Then, the etch conditions change to the overetch (third) step. A long overetch time is required for non-planar MOSFETs to remove completely parasitic polysilicon spacers that form on sidewalls during prior conformal deposition. During this overetch step the gate oxide is exposed, but must not be etched as it protects the underlying source and drain regions. Therefore, a high selectivity of this process to SiO_2 is essential. During the third step, an HBr flow of 70 sccm, an ICP power of $P_{ICP} = 250$ W and an RF power of $P_{RF} = 100$ W have been kept constant, while chamber pressure and O_2 flow have been varied. SiO_2 and polysilcon etch rates have been determined as a function of these parameters. To measure the SiO_2 etch rate silicon samples have been thermally oxidized to a SiO_2 thickness of $t_{ox} = 100$ nm. For the polysilicon samples a polysilicon layer of $t_{poly} = 200$ nm has been deposited by chemical vapor deposition (CVD) on top of the SiO_2.

In Fig. 1(a), the polysilicon etch rate in step 3 (overetch) is shown as a function of oxygen flow for different chamber pressures. The highest etch rate of 64 nm/min is achieved for low oxygen flow and a low chamber pressure of 10 mTorr. As the O_2 flow and the chamber pressure are increased, the polysilicon etch rate decreases (Fig. 1(a)). A similar behavior is observed for the etch rate of SiO_2 in Fig. 1(b) with the highest etch rate of 7 nm/min. For certain conditions, however, SiO_2 etch rates show negative values. This indicates that the etching process stops completely. Instead, chamber condition for plasma enhanced CVD are reached and deposition of SiO_2 occurs. A similar effect has been observed in [7]. For a process without parasitic deposition (O_2 flow of 4 sccm, chamber pressure of 12 mTorr), a selectivity of 100:1 is achieved.

To investigate anisotropy, O_2-flow and chamber pressure have been fixed to 4 sccm and 12 mTorr, respectively. These parameters have been chosen to achieve an extreme selectivity to the oxide at a