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# A hybrid CMOS–SET co-fabrication platform using nano-grain polysilicon wires

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**Abstract**

This paper presents a process for the co-fabrication of self-aligned NMOS and single electron transistors made by gated polysilicon wires. The realization of SET–MOS hybrid architectures is also reported. The proposed process exploits an original low energy "hot" ion implantation for the doping of the 10 nm ultra-thin nano-grain polysilicon wire that serves for building the single electron transistors. Standard MOSFET characteristics and charge trapping, inducing hysteresis in the $I_{DS}$–$V_{GS}$ characteristics of the polysilicon wires, are reported.


*Keywords:* Ultra-thin polysilicon; Hybrid CMOS–SET co-fabrication; "Hot" ion implantation

## 1. Introduction

Recently CMOS–SET hybrid architectures have attracted much attention as they can exploit the virtues of both devices. A combination of CMOS and single electron transistors (SETs) can compensate the limitations of either technology and can bring out novel functionalities [1–3]. SETMOS [2,3] is one such CMOS–SET hybrid architecture, which offers SET-like Coulomb blockade oscillation but at a much higher current level than SET and a unique periodical negative differential resistance effect that could be useful for multiple valued logic application.

In this work, a novel process for hybrid CMOS–SET co-fabrication is proposed and validated. The SET is fabricated using gated polysilicon nanowires with grain sizes of the order of 10 nm and thickness of same order of magnitude. These types of structures have been shown to be interesting candidates for SET devices [4].

## 2. From SET device to SETMOS architecture

The conductive channel in this new single electron device is a polysilicon ultra-thin film (Fig.

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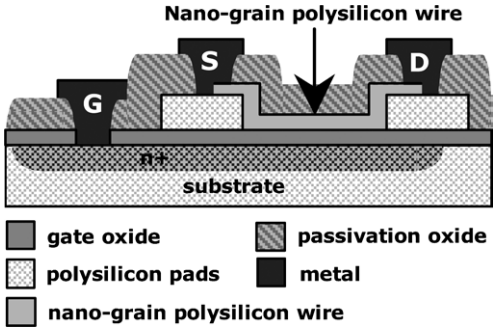


Fig. 1. Schematic cross-section of the fabricated nano-grain polysilicon SET. The device is pseudo-MOS activated by the n-type buried gate. The gate oxide is 40 nm thick and the phosphorous implanted ultra-thin nano-grain polysilicon film is 10 nm. The heavily doped polysilicon pads are used to prevent metal diffusion through the nano-grain film and the underlying gate oxide.

1). The control gate is a highly doped n+ buried layer. Such a simple structure is compatible with the fabrication of NMOS transistors, the resulting process offering a solution to build hybrid CMOS-SET integrated circuits with new functionalities.

Coulomb blockade SET oscillations (well explained by Orthodox theory pioneered by K. K. Likharev [5]) are expected in our polysilicon wires at low temperature. Nano-grains behave like tiny conductive islands connected each other in a network from drain to source (Fig. 2(a)). In order to be sensitive to a few elementary charges this conductive network needs to fulfil the four following engineering challenges: (i) nano-scale size of the width of the nanowire (Fig. 5); (ii) 5–10 nm polysilicon nano-grain size; (iii) conductive dots; (iv) well controlled tunnel barriers between dots. Simulations predict that, when biased, such a film has unique periodic $I_{DS}$–$V_{GS}$ Coulomb blockade characteristics. Some dots are trapping one or few electrons and are behaving as storage dots while other are transfering electrons one-by-one from source to drain by tunneling in a multiple-dots percolation channel. Orthodox theory based simulations allow good prediction of single electron devices characteristics [2], which is needed for circuit design. Monte-Carlo simulated characteristics of a multi-dot ($4 \times 4$) structure, similar to

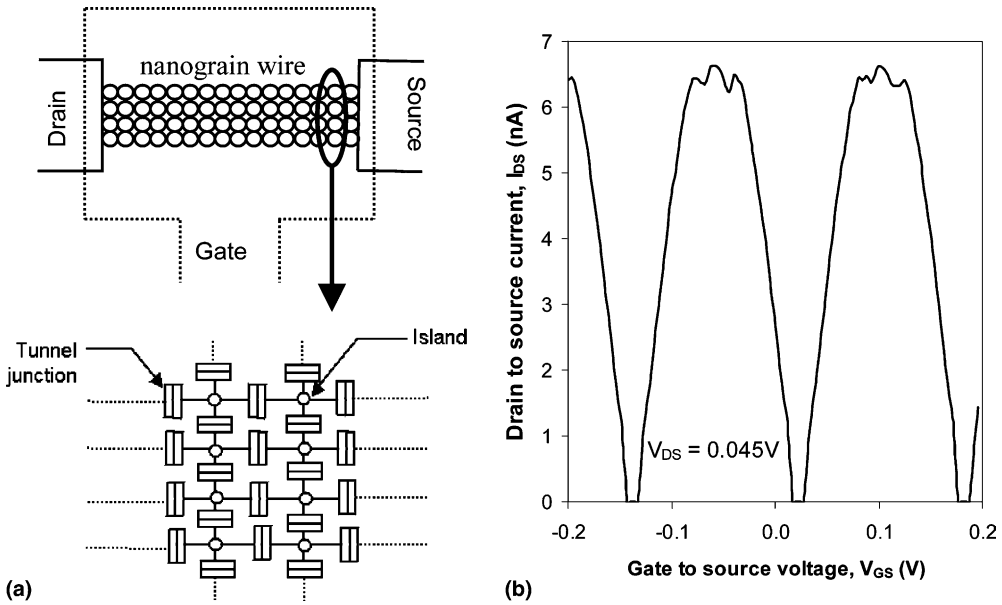


Fig. 2. (a) Physical schematic of the polysilicon nanograin wire used in this work for CMOS–SET co-fabrication. (b) Its Monte-Carlo simulated Coulomb blockade oscillations characteristics (for a $4 \times 4$ nanodots structure). For these simulations, tunnel junction capacitances and gate capacitances are taken to be 1 aF, tunnel junction resistances are 1 MΩ and the operating temperature is 1 K.