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New salicidation technology PtSi for strained SiGe device

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Abstract

To optimize the strained SiGe CMOS process, low temperature salicidate technology is required. In this paper, Pt and Ni have been salicidated at different temperatures and compared. We notice that PtSi yields a lower sheet resistance in general. Furnace and rapid thermal annealing (RTA) have been employed for the salicidation. No big difference for PtSi salicidation occurs for two approaches, RTA is preferable for NiSi salicidation to obtain a lower sheet resistance. The effects of BF^{2+} implantation before salicide junction formed and implantation energy on sheet resistance and contact resistance have been studied. BF^{2+} implantation has no significant effect on PtSi sheet resistance, but it reduces contact resistance dramatically when an implantation energy of 25 keV is used with a dose of 5E15 cm^{-3}. A study of the second thermal step effect on salicidation shows that PtSi has a better thermal stability than NiSi.

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Keywords: Salicidate; Salicidation technology; PtSi; NiSi; Strained SiGe device; Low temperature process; Semiconductor materials

1. Introduction

Strained SiGe CMOS has played an important role in telecommunication [1,2]. Further improvement of its properties for industrial application is drawing intensive attention [3]. One of the improvements is focusing on applying salicide technology to strained SiGe to reduce source/drain resistance and contact resistance [4]. Salicide is one of the indispensable techniques for the high-performance logic devices. Its importance is increasing as the device dimensions go down and hence drain/source sheet resistance becomes larger [5]. $CoSi_2$ has replaced $TiSi_2$ [6], because of its relative stable nature during the salicidation process. NiSi is replacing $CoSi_2$ because of its formation at low temperature and its low sheet resistance with no linewidth dependence [7]. Compared to Ti and Co, NiSi has the lowest silicon consumption

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during salicidation. However, the problems with NiSi are agglomeration at low temperature such as 600 °C and transformation to the high resistivity $NiSi_2$ at 750 °C [8]. We noticed that PtSi has better phase stability, better thermal stability, lower sheet resistance and lower contact resistance compared to NiSi. In this paper, we compared PtSi and NiSi properties and studied the process window by using different salicidation temperatures and different salicidation methods. The thermal stability has been verified by studying the effect of a second thermal step. The effect of BF^{2+} implantation with different implantation energy on sheet resistance and contact resistance is investigated.

2. Experimental

This experiment was designed to investigate the salicidation technologies for strained SiGe CMOS. The strain was found to be relaxed after the temperature reaches 600 °C. Thus, we seek for a salicidation temperature in the range of 300–600 °C. SiGe has always a silicon cap layer for process consumption. This layer may can be used for salicidation. Salicidation may penetrate into SiGe layer because of the thin cap layer. Nevertheless, Silicon salicide will still be the main product even in the SiGe layer. Hence, n-type silicon wafers with nominally 17–33 Ω cm resistivity were employed for this experiment. Metal was thermally evaporated to a thickness of a 30 nm on all the wafers. This was followed by BF^{2+} implantation with a dose of 5E15 cm^{-2} and energies of 25 or 45 keV. Rapid thermal annealing (RTA) and conventional furnace annealing have been used for salicidation. Unreacted metal was then removed by wet chemical etching. Four-probe measurement was performed to characterize the silicide sheet resistance. All the wafers took a second RTA annealing of 30 s at 400 °C in N_2 ambient after the first measurement. Then we measured sheet resistance again to evaluate the thermal stability. The wafers were sawn to a depth of 10 μm to surface isolate 1 mm × 1 mm squares to enable contact resistance to be extract from I to V characteristics.

3. Results and discussion

The sheet resistance of PtSi and NiSi salicided by furnace at different temperature without implantation are shown in Fig. 1(a) and (b) as control samples. The sheet resistance of PtSi and NiSi with BF^{2+} implantation with energies of 45 and 25 keV are indicated as 45 and 25 keV in Fig. 1. A few remarks can be made from this figure, (1) PtSi has a lower sheet resistance compared to NiSi in general. This is understandable because Pt is a better conductor than Ni. (2) BF^{2+} implantation helps to reduce sheet resistance of NiSi, especially with implantation energy of 45 keV and salicided at 300, 400 and 500 °C. This might be explained

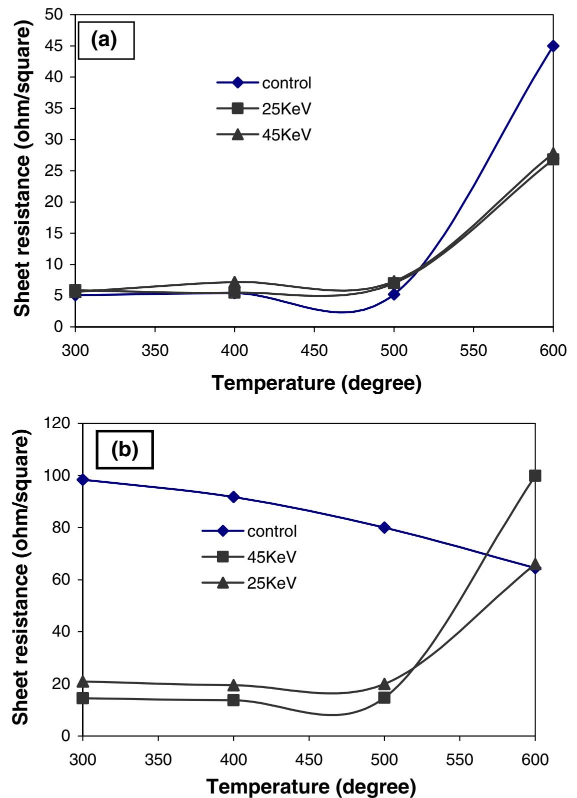

Fig. 1. Sheet resistance of (a) PtSi and (b) NiSi salicided at different temperatures without implantation, indicated as control, and with BF^{2+} implantation with a energy of 25 and 45 keV and a dose of 5E15 cm^{-3}, indicated as 25 and 45 keV, respectively. In general PtSi has lower sheet resistance compared to NiSi.

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