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Silicon nanowires fabricated by means of an underetching technique

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Abstract

Silicon wires with nanometric dimensions have been fabricated on SIMOX wafers by means of e-beam lithography and wet chemical etchings, exploiting the underetching properties of the KOH etchant. The cross section of the resistors has a trapezoidal shape; a minimum top width of 40 nm has been obtained. The whole process required only two writing steps. *I–V* characteristics were measured at room temperature as a function of the backgate voltage.

Keywords: Nanowires; E-beam lithography; Silicon micromachining

1. Introduction

Quantum size effects in the electronic transport through silicon nanowires have been investigated in the last years [1–4] with the aim of designing novel nanoelectronic devices.

Silicon nanowires have been also proposed for other applications such as ultrasensitive bolometers [5] and high sensitive biological and chemical sensors [6], exploiting their good mechanical properties and large surface area to volume ratio.

Two different methodologies have been proposed in the literature for the fabrication of silicon nanowires: (i) a bottom–up and (ii) a top–down approach. The former is usually based on wires grown by means of chemical vapour deposition using Au nanoparticles as catalysts [7,8], while the latter is based on silicon wafer processing by means of high resolution lithography and etching. Typically e-beam lithography on SOI or SIMOX substrates, followed by wet [9,10] or dry [11,12] etching is used. Different fabrication processes,

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employing for example AFM [13] or optical [14] lithography, have been also reported.

In this work, we propose a silicon nanowire fabrication process based on an underetching technique applied to structures defined by e-beam lithography. Wires with a trapezoidal cross section on a SIMOX substrate using a KOH solution as silicon etchant with a top width of about 40 nm were obtained. Preliminary *I–V* characteristics at room temperature and their dependence on the backgate voltage are presented.

2. Fabrication process

The starting material was a SIMOX wafer, ⟨1 0 0⟩ oriented, p doped (10^{15} cm^{-3}) with a 190 nm thick silicon layer insulated from the substrate by a buried SiO_2 layer of 380 nm. A 80 nm thick top layer of SiO_2 was grown by means of thermal dry oxidation at 1000 °C. The structure was defined by means of e-beam lithography (accelerating voltage: 30 kV; dose: about 380 μC/cm^2) using a SEM JEOL JSM-6500F equipped with a purposely built pattern generator [15]. The resist was a double layer of polymethylmethacrylate (PMMA) (996 kMw top layer and 350 kMw bottom layer, 3% in anisole); both layers were spun onto the substrate at 4000 rpm for 30 s and baked on a hotplate at 200 °C for 1 h. After the exposure, the PMMA was developed for 30 s in a solution of three parts of isopropyl alcohol (IPA) and one part of methyl-isobutyl ketone (MIBK) and rinsed in IPA. The patterned PMMA was used as a mask for etching the top SiO_2 layer with a buffered HF (BHF) solution. In Fig. 1(a) a schematic view of the device after the oxide etching is shown: to avoid long e-beam writing times, the mask pattern was a 2 μm wide line. After the resist development, through this mask a trench on SiO_2 film was obtained. To enhance the writing field without mechanically moving the sample, two different writing resolutions during the exposure were used: a high magnification (400×) for writing the central area of the sample, where at the end of the process there will be the wire, and a low magnification (40×) for the periphery.

The silicon layer was then etched with a 35% KOH solution at 45 °C. As known, this solution etches {1 1 1} planes at a much slower rate than the other silicon planes. Aligning the mask edges along the ⟨1 1 0⟩ directions, as shown in Fig. 2, the two oblique sides result oriented in the ⟨1 0 0⟩ directions and so they are rapidly etched while the other sides are limited by {1 1 1} planes. The mask underetching proceeds as schematically shown in Fig. 2, where the solid line is the SiO_2 mask border, the grey area is the plan view of the obtained structure at the end of the silicon etching and the dashed lines are the intermediate steps of the etching process. Thus, the etching time determines the final shape of the etched structure as shown in Fig. 3, where four SEM photos of a sample in temporal sequence, starting with a 5 min etching (Fig. 3(a)) and with steps of 5 min, are reported. As the etching proceeds, the underetching of the SiO_2 mask increases in the direction indicated by the two arrows in figure and the silicon structure dimensions decrease. As shown in Fig. 3(c), a wire laterally limited

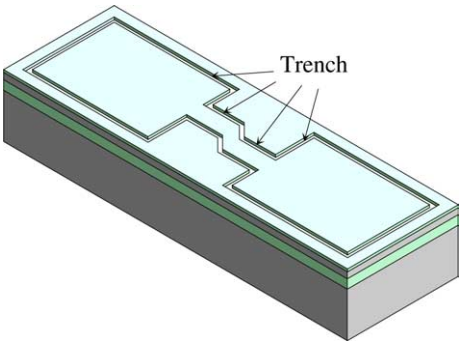

Fig. 1. Schematic view of the structure after the SiO_2 mask definition (not to scale).

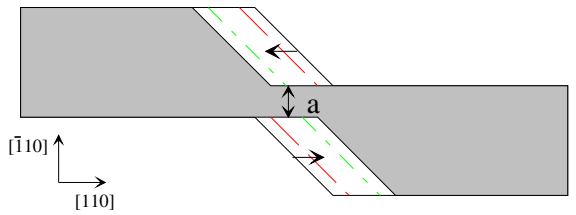

Fig. 2. Plain view of the mask underetching: the two horizontal arrows indicates the Si edge movement during the etching.