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Analysis on the effect of parallel current path on the quality factor of CMOS spiral inductors for 1–10 GHz

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Abstract

A structure of spiral inductor having a parallel current path through the branch of the metal strip was designed to achieve a quality (Q) factor enhancement compatible with conventional CMOS and/or established SiGe process in RF and microwave arena. The Q factor enhanced by 12% was quantitatively analyzed with a lumped-element model and its origin was investigated at a structural point of view. As a result we noted that the parallel-branching structure greatly reduced the series resistance of the inductor at a high frequency range of GHz by suppressing current crowding and in turn enhanced the Q factor beyond the additional parasitic capacitance.

Keywords: Parallel-branch inductor; Quality (Q) factor; Current crowding

1. Introduction

A spiral inductor, one of the most problematic devices due to its low quality (Q) factor among the passive devices in a design of silicon RF and/or microwave integrated circuits, has been extensively investigated from the viewpoint of various fabrication methods at several frequency bands. It was conceptually stated by Yue et al. [1] that the Q factor of a spiral inductor is determined by the competition between an inductive component of the metal strip and a parasitic one of the lossy substrate as expressed in Eq. (1) [1,2]

$$Q = \frac{\omega L_S}{R_S} \cdot \frac{R_P}{R_P + [(\omega L_S/R_S)^2 + 1]R_S} \cdot \left[1 - \frac{R_S^2(C_S + C_P)}{L_S} - \omega^2 L_S(C_S + C_P)\right], \quad (1)$$

where R_S, C_S, L_S are series resistance, capacitance, and inductance of the metal strip while R_P and C_P parasitic resistance and capacitance of the lossy

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substrate including dielectric layer, respectively. The Q factor expressed by Eq. (1) generally shows a convex parabolic shape in the range of 1–10 GHz where the upward and downward segments are dominantly governed by the resistive and the capacitive components of the inductor, respectively [1].

There have been two prior approaches for the enhancement of Q factor; one is to reduce the resistive component of the inductor itself and the other to reduce the parasitic components of the lossy silicon substrate. As for the former approach the material of the metal strip is now shifting from aluminum to lower resistance materials such as copper or silver [3] in pursuit of the leverage of thick metallization [4,5]. As for the latter approach the guard-ring technique [1] that suppresses the parasitic current in silicon substrate was introduced although the shielding effect is questionable from a practical point of view. However, both approaches are accompanied with substantial difficulties in both process cost and productivity as far as the spiral inductor is fabricated using a standard silicon process.

In the present paper we designed a new Q-enhanced spiral inductor on silicon through the adoption of electrically parallel circuit. We implemented the simplest parallel current path of a spiral inductor with aluminum on low resistive silicon that is a severe environment for a high frequency inductor and analyzed the enhanced Q factor. Eventually we explained the superiority of the Q factor of the parallel-branch inductor to the conventional one of the same dimension and inductance.

2. Experimental

A conventional inductor and the present parallel-branch inductor were simultaneously prepared on the same p-type silicon substrate (ρ = 5–15 Ω cm) as shown in Fig. 1(a) and (b). Both are squared spiral inductors having silicon dioxide of 1 μm-thick as an insulating layer. The dimensional specification of the inductors and the substrate were summarized in Table 1. The upper metal strip of the conventional inductor was connected only once with the lower one through one via whereas the upper metal strip in the parallel-branch was connected with the lower one through several vias as shown in Fig. 1(a) and (b). So in the parallel-branch inductor input current goes into the upper strip initially and finally comes out of the very upper strip after several branching-offs and joining again at the vias. In addition, the branching structure was designed to make all segments of the lower strip spiral parallel to those of the upper one for the sake of maximum inductance. Although the additional lower strip might increase the parasitic capacitance and in turn to reduce the Q

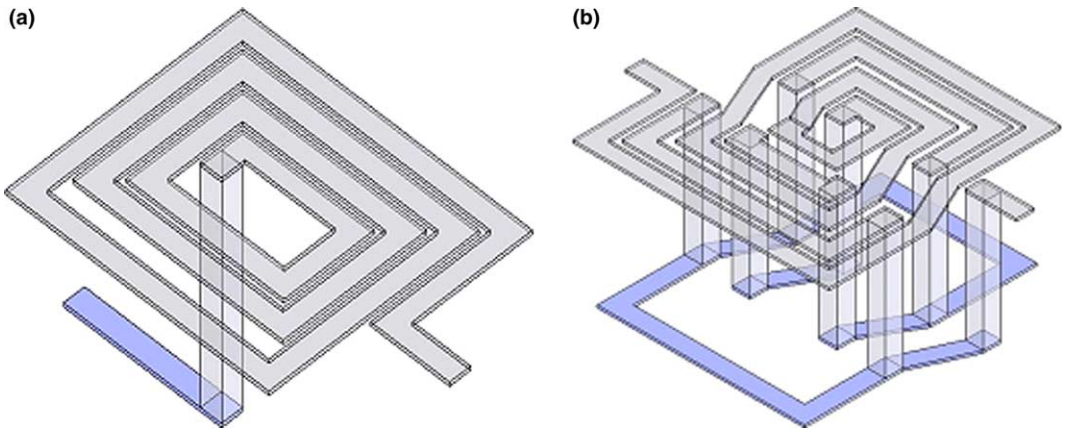

Fig. 1. Schematic diagrams of (a) the conventional and (b) the parallel-branch inductors.