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Charge trapping in MOSFETs with HfSiON dielectrics during electrical stressing

Robert O'Connor [a,*], Greg Hughes [a], Robin Degraeve [b], Ben Kaczer [b]

[a] School of Physical Sciences, Dublin City University, Collins Avenue, Glasnevin, Dublin 9, Ireland
[b] IMEC, Kapeldreef 75, B3001, Leuven, Belgium

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Abstract

Hafnium silicate had been suggested as a possible 'mid-*k*' alternative to SiON as a gate dielectric for the 45 nm technology node. This work focuses on the shift in threshold voltage, the degradation in transconductance, and the subthreshold swing during oxide stress. Analysis of these parameters reveals much about the trap generation mechanisms in the layers, as well as differences from SiON. The effect of the aspect ratio dimensions on post-breakdown device functionality is also discussed.

Keywords: Hafnium silicate; High-*k*; Reliability; Charge trapping

1. Introduction

In the scaling of MOSFETS, the gate dielectric plays a critical role, and an extensive range of papers exist on the subject of estimating the lifetime and integrity of these layers as they become thinner and are subjected to ever increasing current densities and electric fields [1–3].

The need for a 'high-*k*' layer to replace SiO_2 as the dielectric layer in scaled MOSFET devices to stem the leakage current problem is evident. Metal oxides such as HfO_2 are desirable because of their extremely high (~40) dielectric constant, but suffer from problems such as reduced mobility [3] and threshold voltage instability due to charge trapping. One possible solution is not to move entirely away from Si-based dielectrics, but to use silicates, which form a more stable interface with silicon. The majority of the literature on the topic of dielectric breakdown is based on the ability of the layer to withstand breakdown for the specified operating lifetime [4]. Earlier work has shown that the time to breakdown of the layers in this study is approximately 10 years at operating voltage using

* Corresponding author. Tel.: +353 1 7005978; fax: +353 1 7005384.
E-mail address: roc@physics.dcu.ie (R. O'Connor).

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a linear extrapolation and so the reliability condition is attained. However, it is necessary to take into account the possibility of devices continuing to function well into the 'progressive breakdown' regime as exhibited by very thin oxide layers [5]. This effectively means that extra time could be legitimately added to a reliability estimate. There is also the possibility that threshold voltage shifts and mobility degradation before the breakdown of the oxide, and this could be the determining factor in defining device reliability.

This work demonstrates that the silicate layers investigated in this study have an unacceptably high threshold voltage shift during stress measurements and that even though transistor structures based on these layers continue to satisfactorily function during the progressive breakdown stage, the high threshold voltage shift and the transconductance degradation effectively mean that the devices fail to meet operational specifications.

2. Devices and experiments

The devices used for these experiments were *n*-MOSFETs with areas from 10^{-4} to 10^{-8}cm^2. The wafers were initially prepared by carrying out an IMEC clean on the silicon surface. Following this, the HfSiO layers were grown by MOCVD with SiO_2 and HfO_2 resulting in HfSiO thicknesses in the range of 1.0–3 nm. Then, to stabilize the layer, a post deposition anneal was carried out in a NH_3 atmosphere at 800 °C for 1 min. The processing sequence used has led to thicknesses of 1.53–2.14 nm Equivalent Oxide Thickness (EOT). The layers were shown to have a lower leakage current than SiON of similar EOT (Fig. 1) and to have similar time-to-breakdown in a reliability study.

To evaluate the functionality of *n*-MOSFETS during a CVS or CCS, transistors of various channel lengths (10–0.25 μm) and widths (10–0.25 μm) were studied. The study consisted of acquiring an I_dV_g curve and a set of characteristic I_dV_d curves at a variety of gate voltages and examining the ratio of on-state and off-state currents. From the set of I_dV_g curves (Fig. 2) taken as a function of increasingly long voltage stress times, the change

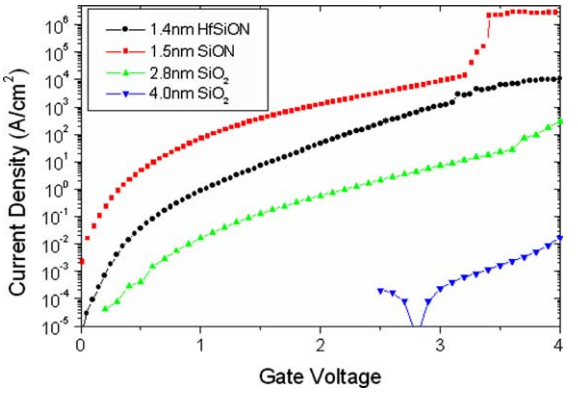

Fig. 1. *IV* curves for HfSiO and more conventional oxides. The HfSiO has a lower leakage current than a SiON sample of similar EOT.

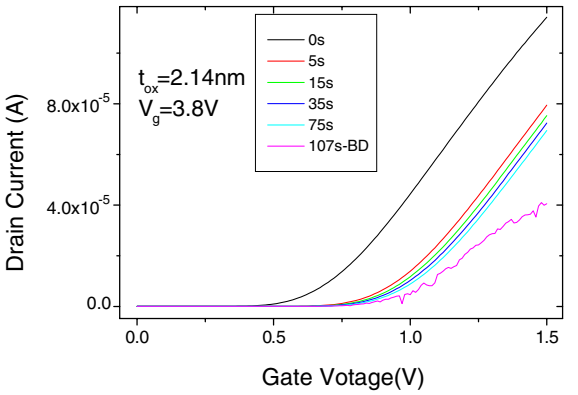

Fig. 2. A set of I_dV_g curves during constant voltage stress. The curves are seen to shift to the right, leading to an increase in threshold voltage. V_D = 1.2 V.

in threshold voltage, transconductance degradation and the sub-threshold swing can be evaluated. By monitoring I_{on} and I_{off}, we can also evaluate the functionality of the device during oxide degradation into the post breakdown wear-out phase and examine the impact of device aspect ratio.

The on-state current is the drain current (I_d) with a drain-source voltage (V_{ds}) equal to four times the threshold voltage and the same voltage applied to the gate. The off-state current is (I_d) with (V_{ds}) equal to four times the threshold voltage and gate voltage = 0. After acquiring the parameters I_{on} and I_{off} from the curves mentioned above, the gate oxide was stressed at high field. The stress