Available online at www.sciencedirect.com
SCIENCE DIRECT®
Microelectronics Reliability 45 (2005) 437–455
MICROELECTRONICS RELIABILITY
www.elsevier.com/locate/microrel

Introductory Invited Paper

A review of CMOS latchup and electrostatic discharge (ESD) in bipolar complimentary MOSFET (BiCMOS) Silicon Germanium technologies: Part II—Latchup

Steven H. Voldman *

Silicon Germanium Development, Semiconductor Research and Development Center (SRDC), IBM, 1000 River Street, MS 972F, Bldg 972-1 Col A8, Essex Junction, VT 05452, United States

Received 5 November 2004
Available online 8 January 2005

Abstract

CMOS latchup and electrostatic discharge (ESD) continue to be a semiconductor quality and reliability area of interest as semiconductor components continue to be reduced to smaller dimensions. The combination of scaling, design integration, circuit performance objectives, new applications, and the evolving system environments, CMOS latchup and ESD robustness will continue to be a technology concern. With both the revolutionary and evolutionary changes in CMOS and Silicon Germanium semiconductor technologies, and changing product environments, new CMOS latchup and ESD requirements also continue in semiconductor design, device and chip-level simulation, design verification, chip-to-system evaluation, and the need for new latchup and ESD test specifications. Additionally, the issues of low cost, low power and radio frequency (RF) GHz performance objectives has lead to both revolutionary as well as derivative technologies; these have opened new doors for discovery, development and research in the area of latchup and ESD. Although latchup and ESD are not a new reliability arena, there are also new issues rising each year, making the latchup and ESD an area of continuous discovery, innovation and invention. In this paper, an introduction to latchup in CMOS and BiCMOS Silicon Germanium will be discussed.

1. Introduction

In the 1970s early work on CMOS latchup was underway for space applications [1,2]. In the early 1980s, CMOS latchup and electrostatic discharge (ESD) phenomenon of significant interest; the reason for the significant interest in CMOS latchup and ESD was driven by the fact that CMOS latchup and ESD was a significant reliability concern [3–8]. Gregory and Shafer's work was one of the early publications that addressed the introduction of CMOS as a mainstream technology, and the CMOS latchup problem [3]. One of the reasons that there was a growing interest was because complimentary metal oxide semiconductor (CMOS) technology, and CMOS latchup was a roadblock to mainstream introduction of CMOS technology [1–9]. In the early 1980s, in many semiconductor suppliers, there was a lack of understanding, semiconductor process solutions, test structures, standards, models, simulations, design methodologies, design rules, and design checking and verification systems to address the CMOS latchup concern. To contain the CMOS latchup

* Tel.: +1 802 769 8368; fax: +1 802 769 9659.
E-mail address: a108501@us.ibm.com

0026-2714/$ - see front matter © 2004 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2004.12.001

issue, development engineers and researchers began to build a successful labyrinth of technology solutions, processes, design rules and practices [3–9]. Estreich's thesis work at Stanford University moved the subject forward to address practical issues and models [7]. It was also at this time frame, the book by Troutman, "Latchup: The Problem and The Cure" acknowledged a state of understanding and conquering the problem [9].

In the late 1980s and early 1990s new semiconductor processes further enhanced the CMOS latchup robustness of the mainstream CMOS technologies [9–20]. In CMOS technology, semiconductor process solutions were integrated to improve the CMOS latchup issue. Heavily doped p^{++} substrates were added to CMOS memory and logic technologies to improve both the CMOS latchup robustness and the soft error rate (SER) concerns [14,15]. Retrograde n-well implants were integrated to lower the shunt resistance in single well CMOS technology [14–19]. In 1983, Troutman first introduced a retrograde well using a high energy MeV implanter into a mainstream CMOS technology (IBM's CMOS IV 0.8 μm technology). Voldman and Cottrell addressed the issues of retrograde well optimization, integration and latchup in the 0.8 μm CMOS technology (1984) [14]. Voldman addressed retrograde well, epitaxy optimization and latchup in the first CMOS technology that introduced shallow trench isolation (STI) technology—IBM's 0.5 μm CMOS technology (1992) [15–18]. Shallow trench isolation (STI) replaced the shallower LOCOS isolation structure further improving the CMOS latchup robustness of the technology [18]. P-well regions were formed in the epitaxial region in dual well CMOS technology [19]. New concepts, such as heavily doped buried layers (HDBL) and buried guard ring (BGR), as proposed by Morris, as alternative processes were also demonstrated as a latchup solution [20]. In the 1980s, Troutman established design test structures which became industrial standards for CMOS latchup benchmarking semiconductor technologies. Latchup design practices, such as guard rings, and double guard rings were added into design methodologies to isolate the p-channel and n-channel MOSFETs in off-chip driver circuits. Single- and double-guard ring rules were also established to isolate injecting sources of minority carriers. New design tools were developed to identify parasitic pnpn structures for design verification and checking. These directions gave us more confidence that the CMOS latchup problem was solved.

With the continued scaling of physical dimensions, to preserve dimensional similitude as well as provide manufacturability, the vertical profile is scaling with the lateral dimensional scaling [19,20]. With the lateral scaling, the vertical scaling of junctions, p-wells, n-wells, and isolation depth is occurring. In the case of well scaling, the well depths are decreased; this leads to the lowering of the doping concentration and implant dose will require to be reduced in order to maintain low capacitance, and low leakage MOSFET junctions. Hence, the vertical dimensional scaling impacts both the energy and dose of the well implantation. For example, in the 0.5-μm CMOS technology generation, shallow trench isolation (STI) was introduced; but with the continued scaling of technology, the STI depth decreased accordingly with the vertical profile scaling.

During this time frame, other issues were also changing the direction of semiconductor processes and chip design. With the increase in circuit density, with digital networks, the peripheral circuits were required to separate from the core networks because of noise and switching concerns. Noise isolation is also necessary between digital and analog circuits in a mixed signal chip environment. With the addition of radio-frequency (RF) circuits, the digital, analog and the RF networks require separate power grids and noise isolating structures. As a result, the trend in semiconductor technology is to go to higher substrate resistance with technology scaling and higher integration.

Additionally, mixed voltage applications require power supply voltage conditions well above the native CMOS power supply voltage of the semiconductor technology. Mixed voltage interface peripheral receiver circuits typically must interface with the voltage of the external system whose voltage is above the native voltage of the semiconductor chip. Second, bipolar and BiCMOS circuits typically will have power supply voltages that exceed the native CMOS core logic. Bipolar and BiCMOS applications will also have a positive power rail, V_{CC}, ground rail V_{SS} and negative power rail V_{EE}, which leads to a larger voltage differential between the V_{CC} and V_{EE}. Where mixed voltage applications existed in prior technology generations, the present generations have a lower voltage margin to CMOS latchup.

Today, system level conditions are more flexible compared to older systems. Power-up, and power-down conditions have been changing to allow increase system portability and flexibility. The power-up and power-down of system components are today more prevalent, as well as hot plugging conditions. Cable insertion for electrical connections for phone lines, web access, Ethernet, mice and power supplies have increased as well as the number of cables. As a result, charged cable events are more prevalent leading to CMOS latchup events [21].

Today, in advanced CMOS and BiCMOS Silicon Germanium technology, highly scaled circuits are integrated in mixed signal applications for chip and circuit performance. As a result of the dimensional scaling and integration issues, the CMOS latchup sensitivity is higher than prior generations. As a result of the CMOS scaling, latchup must be addressed.

In BiCMOS technology, many features as well as old and new processes that open the opportunity to improve