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Characterization of bump arrays at RF/microwave frequencies

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Abstract

A systematic procedure for the characterization of complex bump configurations at RF and microwave frequencies, is presented. Beginning with simple arrangements—single- and two-coupled bumps—full-wave electromagnetic (EM) field analysis, circuit simulations and RF measurements were used for the development and validation of their respective equivalent circuit models. These models were then extended to characterize three-coupled bumps, both in linear and triangular configurations. Finally, a combination of all the electrical parameters obtained from these simple bump configurations was used to characterize a complete bump array, taking into consideration that for pitches used in most high-speed packages, EM coupling between a bump and its "next but one" neighbor can be neglected.

1. Introduction

Improved electrical performance, higher I/O count for a given substrate area, reduced component size, cost and weight, are just a few of the myriad of advantages offered by area-array packages (e.g., flip chip, BGA, ...) over peripherally leaded packages. Most of these advantages arise mainly due to the use of bumps for signal transmission either between the chip and its carrier and/or carrier and the board (e.g., PCB, ...). However, since these bumps are mostly designed in an area-array configuration so as to increase the signal density, an interaction of their EM fields often results to signal degradation effects, that can limit the system performance, especially as operating frequencies continuously move up the microwave band. Hence, thorough electrical characterization of bumps in such configurations is a prerequisite for an effective design of area-array packages.

Although there have been numerous publications on flip chip interconnects in recent years, (e.g., [1–6]), the focus has been mainly on the characterization and optimization of a single bump.

In this contribution, however, a systematic procedure for the characterization of complex bump arrangements at RF and microwave frequencies is presented. Our approach commences with the definition of a design space for these bumps, followed by full-wave EM field analysis. First of all, lumped element models for a single bump and two-coupled bumps were extracted from the field simulations and validated using RF measurement of test structures. These models were then extended to characterize a configuration of three-coupled bumps. Finally, a complete bump array was characterized using only electrical parameters extracted from a single bump and two-coupled bumps (placed in parallel and diagonally).

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2. Systematic procedure

For typical bump pitches used in most high-speed packages, EM coupling between a bump and its "next but one" neighbor can be neglected. Neglecting this coupling and considering the symmetrical arrangement of bumps, leads to a considerable reduction in the number of parameters to be extracted when accounting for the electrical behavior of bump arrays at RF and microwave frequencies [7]. For an illustration of this technique, an array of flip chip interconnects (bumps), schematically shown in Fig. 1, was used as an example, and the following procedure was implemented:

- An equivalent circuit model for a single flip chip interconnect was first derived. As it will be seen later in the text, this interconnect can be completely characterized by its resistance (R) and inductance (L). These electrical parameters can be used to characterize any other interconnect in the array configuration, since all flip chip interconnects in such an arrangement are geometrically and materially the same.
- Secondly, a circuit model for any two nearby interconnects was developed and their coupling parameters—mutual inductance (M) and coupling capacitance (C)—were extracted. Depending on whether the interconnects are placed in parallel or diagonally to each other, these coupling parameters are shown as M_p, C_p and M_d, C_d, respectively, in Fig. 1.
- Coupling parameters extracted from two parallel bumps (e.g., between B1 and B2 or B1 and B4) were used to characterize a linear arrangement of three-coupled bumps having a pitch of 100 μm. Using this bump configuration, as an example, it was also proven that EM coupling between a bump and its "next but one" neighbor can be neglected.
- Finally, a complete bump array was characterized using only electrical parameters extracted from a single bump and two-coupled bumps.

In the following sections, an elaboration of the systematic procedure implemented will be presented.

2.1. Electrical modeling of a single bump

The flip chip interconnect used in this work has a height and diameter of approximately 50.8 μm and a conductivity of 6.70E + 06 S/m. As it was previously mentioned, this interconnect can be completely characterized by its resistance and inductance. In order to extract these parameters, parameterized equations for a single bump, developed and validated in [8], and presented below, were used.

$$\begin{aligned} L[H] &= f(JH, D1, D2) \\ &= a_0 + a_1 JH + a_2 D1 + a_3 D2 + a_4 JH \cdot D1 \\ &\quad + a_5 JH \cdot D2 + a_6 D1 \cdot D2 + \ldots \end{aligned} \tag{1}$$

$$\begin{aligned} R[\Omega] &= f(JH, D1, D2) \\ &= a_0 + a_1 JH + a_2 D1 + a_3 D2 + a_4 JH \cdot D1 \\ &\quad + a_5 JH \cdot D2 + a_6 D1 \cdot D2 + \ldots \end{aligned} \tag{2}$$

where JH is the bump height, $D1$ and $D2$ are the chip and substrate pad diameters, respectively. The coefficients, a_i, were estimated by adequate statistical algorithms, and eventually validated by statistical methods, test simulations and test sample checks [8].

For the development of these equations, a DOE (Design of Experiment) was set up and full-wave EM field simulations of 3D models of a single-bumped flip chip (see Fig. 2) were performed using Ansoft's HFSS, in a frequency range of 1 GHz to 30 GHz. Based on the field simulation results, an equivalent circuit model (as shown in Fig. 3) was developed. Each element in this equivalent

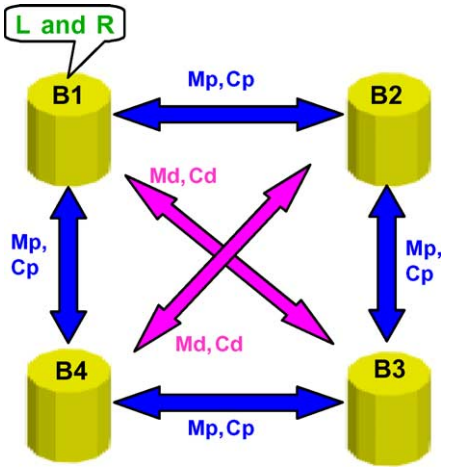

Fig. 1. Schematic representation of an array of flip chip interconnects.

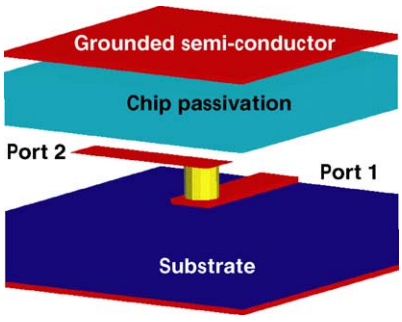

Fig. 2. EM model of a single-bumped flip chip.