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Silicon-on-diamond: An advanced silicon-on-insulator technology

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Abstract

Silicon-on-diamond (SOD) technology is proposed as an advanced alternative to conventional silicon-on-insulator (SOI) technology. In SOD, the electrical insulator is diamond, the best thermal conductor in nature. In our SOD concept, the diamond film is highly oriented (HOD), 75–100 μm thick and serves as an electrical insulator, heat spreader and substrate. In this paper, we focus on the thermal evaluation of SOD with a Si device layer on the nucleation side of the diamond film. The obtained results indicated that SOD can sustain up to 10-times higher power loads than SOI. The results were experimentally obtained by $R(T)$ measurements of micro-heaters deposited on the Si device layer and by thermal imaging. 3D finite element thermal simulations using ANSYS confirmed that these numbers are in good agreement with expectations.

Keywords: Silicon-on-diamond (SOD); Heaters; IR-imaging; 3D-FE

1. Introduction

In the past, the development of Si technology has been well predicted by Moore's law [1], which projects an exponential growth of the number of devices on a chip over time. However, continuous growth will soon encounter major barriers associated with the physical properties of the materials. One of the biggest challenges is thermal management. The International Technology Roadmap for Semiconductors (ITRS) projects that for 2005–2009 the maximum junction temperature in high-performance chips will be 85 °C [2]. According to Ref. [3] and the ITRS, solutions for heat removal in future IC's are not yet known.

One alternative to classical CMOS technology is SOI, since it enables lower overall operating powers. With respect to the bulk Si, IC's utilizing SOI show a performance gain of 30% at identical feature sizes [4]. The only advantage of SOI is the electrical isolation provided by the SiO_2. However, as the device density in IC's continues to increase [5], the poor thermal conductivity of the SiO_2 represents a major drawback.

Clearly, the substitution of SiO_2 with electrically insulating, high thermally conductive diamond, i.e. the substitution of SOI with SOD represents a promising alternative. Annamalai et al. were the first to successfully fabricate SOD and Si-MOSFETs on SOD [6–8]. Fabrication of MOSFETs using a similar SOD structure was also reported by Soderbarg et al. [9–11] and transferred to a 4 in. Si-substrate by Gu et al. [12]. In these initial SOD demonstrations, a thin (2–3 μm) diamond film was sandwiched between a thin Si-device layer and a thick Si-wafer. However, we believe that this SOD concept is ultimately limited by the material properties and thermal management capabilities of the bulk Si. In addition, it is well documented that the thermal conductivity of diamond increases with the grain size [13], and is quite small for thin films below 10 μm. From all the previous studies of SOD mentioned above, only in [9] was there calculated a 2D heat distribution for a point heat source in SOD with respect to SOI. Experimentally the operating temperatures for diodes fabricated on SOD were compared with respect to devices on SOI, and it was found that temperature excursions were 3–4 times lower for SOD.

In the SOD concept proposed here, see Fig. 1a, the SOD wafer is a diamond film/substrate adjoined to a thin single

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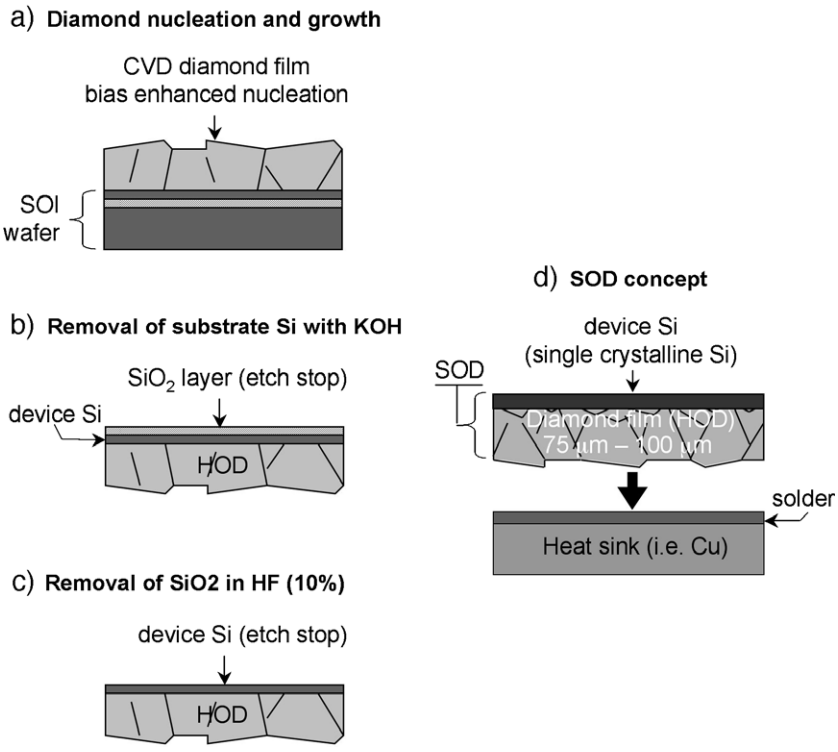

Fig. 1. (a–c) Fabrication of the SOD wafer, d) the SOD concept.

crystal Si layer on one side. The diamond is thicker and is no longer sandwiched between Si layers. In practice, the Si-device layer can be situated either on the nucleation side of the diamond film (SOD-N) or on the growth side of the diamond film (SOD-G). For this study only SOD-N samples were investigated. The polycrystalline diamond film used in this concept is highly oriented (HOD) [14,15]. HOD was used in this study because it has nearly twice the thermal conductivity of randomly-oriented polycrystalline diamond of the same thickness [16]. The thermal conductivity of these diamond films is greatest perpendicular to the growth/nucleation surface, which in the proposed structure provides for effective extraction of the heat away from the active channel to the heat sink on the opposite side of the film [17].

In this work, the thermal management properties of SOD-N with respect to SOI and Si are measured experimentally by monitoring temperature dependent changes in the resistivity of metal strip heaters and by IR-thermal imaging. 3D finite element thermal simulations provided a complementary theoretical prediction for the heat distributions in SOD and SOI.

2. Experimental

2.1. Fabrication of SOD-N wafers

The fabrication of the SOD samples is illustrated in Fig. 1b–d. First, an HOD film is grown on commercial (100) SOI wafers, characterized by a 1.5 μm thick Si device layer, 3.0 μm of SiO_2 and a 525 μm thick Si substrate. The wafers were sectioned to be accommodated in the diamond growth system. The nucleation/growth procedures for HOD on SOI were the same as described in [14,15] for HOD on Si. Diamond nucleation on the Si-device layer of the SOI wafer section was achieved by in situ Bias-Enhanced Nucleation (BEN). For effective nucleation on the Si-device layer, a conducting bypass of the SiO_2-layer for the bias potential was provided by inducing an electrical short between the Mo sample holder and the top surface of the SOI wafer section using Mo-foil. Following the diamond growth, the Si substrate was etched away in 6 M KOH using the SiO_2 layer as an etch stop. The SiO_2 layer was then etched in 10% HF, with the device Si serving as an etch stop, to provide the final SOD wafers. This technology resulted in the fabrication of SOD wafers with device grade Si in just 3 technological steps (diamond nucleation + growth, a wafer Silicon etch and a SiO_2 etch). In addition, only the initial nucleation step of diamond has the potential of damaging the Si device layer. In fact, no change in the morphology of the Si device layer was observed after SOD fabrication and preliminary X-ray diffraction measurements indicate that the device Si of the SOD wafer is of the same quality as the device Si layer on the original SOI wafers.

The only possible drawback of this technology is the roughness of the wafer backside, i.e. the growth side of the diamond film. However, the roughness of HOD is only on the order of the standard backside roughness of semiconductor grade Si wafers. This is not detrimental regarding wafer handling and would permit the use of a solder bond as