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Separation by bonding Si Islands (SBSI) for LSI applications

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Abstract

We propose and describe a novel method called separation by bonding Si islands (SBSI) that can be used to form silicon-on-insulator (SOI) and isolation regions simultaneously. The Si islands are formed by selectively etching the SiGe layer of Si/SiGe stacked layers grown by chemical vapor deposition (CVD). Thin oxide layers are formed at the surface of the Si islands and the Si substrate by using thermal oxidation, and the Si islands are bonded to the Si substrate with the oxide layers. We obtained a uniform SOI layer and a smooth interface between the SOI and buried oxide (BOX) layers. The thicknesses of the SOI and BOX layers observed with cross-sectional transmission electron microscopy (TEM) were 18.2 and 23.5 nm, respectively.
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1. Introduction

Recently, the demand for CMOSs fabricated on silicon-on-insulator (SOI) substrates has been increasing because high-density devices that operate at high speed with low power consumption can be realized. In addition, the SOI and buried oxide (BOX) layers are being made thinner because of the reduced size of the devices, and forming the layers at less than 20 nm will be required in the near future [1]. Moreover, various methods are used for fabricating the SOI substrates, such as separation by implanted oxygen (SIMOX) [2], ELTRAN® [3], and Smart-cut® [4]. These methods have brought about excellent device performance due to the high quality of the SOI and BOX layers. However, much work is required to meet the above-mentioned demand for the thinner layer thicknesses.

In this paper, we propose and describe a novel method called separation by bonding Si islands (SBSI) [5] that can form SOI and isolation regions simultaneously. The Si islands are formed by selective etching of the SiGe layer of Si/SiGe stacked layers grown by chemical vapor deposition (CVD), and bonded to the Si substrate with the thermal oxide layers formed at the surface of the Si islands. In the proposed method, the SOI and BOX layers are formed by CVD and thermal oxidation, respectively. Therefore, these layers can be thinner and more precisely controlled than those formed using conventional meth-

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ods. We also investigated the selective etching of the SiGe layer for cap-Si/SiGe stacked layers grown on Si substrate to form thin and uniform Si islands.

2. Separation by bonding Si islands

Fig. 1 shows a schematic of the fabrication procedure of for the SBSI process. First, SiGe and cap-Si layers are grown on Si(1 0 0) substrate by CVD. Then, the Ge content must be controlled so as not to increase defect density in the cap-Si layer. This is necessary because the strain in the SiGe layer increases with Ge content so that a higher Ge content would generate defects in the cap-Si layer grown on the SiGe layer.

Following the growth of the cap-Si/SiGe layers, trenches are formed followed by the deposition of a non-doped CVD-SiO_2 (Fig. 1(b)). Next, the CVD-SiO_2/cap-Si/SiGe layers are etched after photo-resist patterning (Fig. 1(c)). Then, only the SiGe layer is selectively etched by a solution composed of HF and HNO_3 after photo-resist stripping (Fig. 1(d)). Next, thin oxide layers are formed via thermal oxidation at the surface of the Si island and the Si substrate (Fig. 1(e)). Subsequently, furnace annealing is performed to reflow the CVD-SiO_2, and then the Si island with the oxide layer is bonded to the Si substrate (Fig. 1(f)). Finally, the trenches for the isolation region are filled with CVD-SiO_2 with a chemical mechanical polishing (CMP) process (Fig. 1(g)).

3. Selective etching characteristics of SiGe layer

To form the thin and uniform Si island shown in Fig. 1(d), a highly selective etching of the SiGe/Si is necessary. Therefore, we investigated selective etching of the SiGe layer for the cap-Si/SiGe layers grown on Si substrate. The experimental procedure was as follows. First, boron-doped $Si_{0.67}Ge_{0.33}$(10 nm) and cap-Si(70 nm) layers were grown on a chemically cleaned HF-last p-Si(1 0 0) substrate by using an ultraclean hot-wall LP-CVD system [6] at 500 and 550 °C, respectively. As source gases, SiH_4-GeH_4-B_2H_6 were used for the SiGe layer and SiH_4 was used for the cap-Si layer. The total growth pressure for the SiGe layer and the cap-Si layer were 30 and 12.5 Pa with H_2 and Ar as a carrier gases, respectively. We measured the boron doping concentration of the SiGe layer with secondary ion mass spectrometry (SIMS) and found that it was approximately $10^{19}\,cm^{-3}$. Following the growth of the cap-Si/SiGe layers, a non-doped CVD-SiO_2 was deposited at 400 °C as a passivation layer. After the photo-resist patterning, the CVD-SiO_2 layer and the cap-Si/SiGe layers were etched using a buffered hydrofluoric (BHF) acid and a plasma-etching system. After that, the sample was dipped into a DHF acid to remove the native oxide after the photo-resist stripping, and then the SiGe layer was etched laterally with HF(50%):HNO_3(61%):-H_2O = 1:120:60.

Fig. 2 shows a cross-sectional scanning electron microscopy (SEM) image after the selective etching of the SiGe layer. The SEM observation revealed that only the SiGe layer was selectively etched, and it was confirmed a high etching selectivity of the SiGe layer against the Si. Furthermore, the laterally etched length was about 0.44 μm for 60 s, and this length was sufficient for fabricating the devices on the cap-Si layer that would become the SOI layer.

It is also important to retain a smooth surface after the etching of the SiGe layer to form a smooth interface between the Si island and the thermal oxide layer as shown in Fig. 1(e). Fig. 3 shows the dependence of the

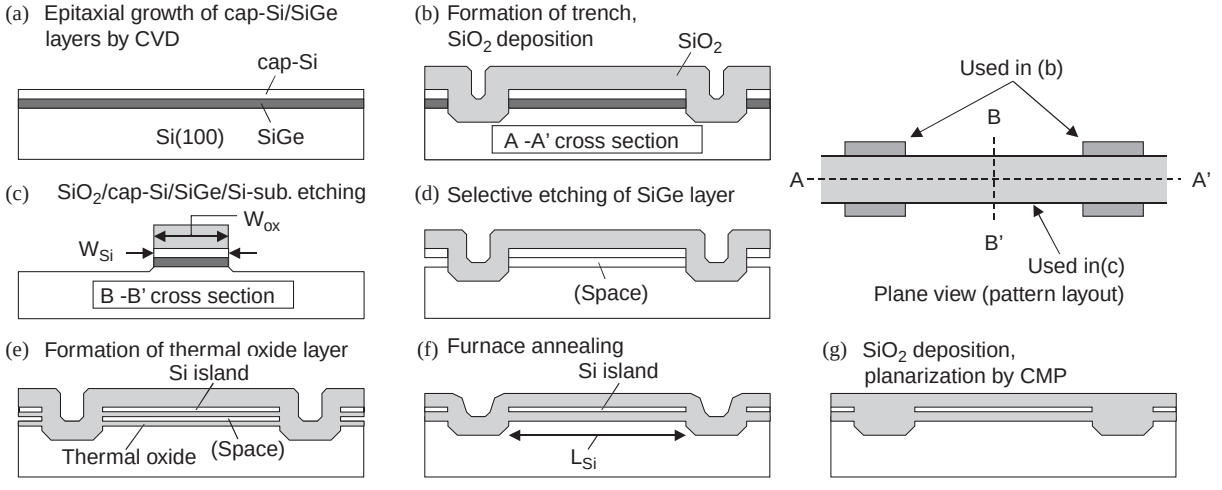

Fig. 1. Schematic fabrication procedure of separation by bonding Si islands (SBSI) process.

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