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Misfit dislocation nucleation and multiplication in fully strained SiGe/Si heterostructures under thermal annealing

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Abstract

An evolution of dislocation structure formed in fully strained $Si_{1-x}Ge_x/Si(0\,0\,1)$ heterostructures during thermal annealing was studied. Heterostructures with Ge content $x = 0.15$ and 0.30 were grown by MBE on low-temperature Si(400 °C) and SiGe(250 °C) buffer layers. The main attention was devoted to the initial stages of strain relaxation and to the role of intrinsic point defects in misfit dislocation nucleation. A mechanism is proposed for the misfit dislocation nucleation at heterogeneous sources placed within SiGe epitaxial layer.

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1. Introduction

Fully strained heterostructures containing epitaxial layers enriched with intrinsic point defects are currently used for preparing SiGe/Si virtual substrates. Thermal annealing of such heterostructures leads to practically full strain relaxation even in the case of thin buffer layers (<200 nm) [1–4]. However, low threading dislocation density ($\leqslant 10^5\,cm^{-2}$) cannot always be obtained in these layers. This problem stimulates further investigations of the processes of misfit dislocation (MD) nucleation, propagation and multiplication.

A lot of mechanisms of MD generation have been suggested by now (see, for example, a review [5]). Most part of these mechanisms is based on the formation of spiral or Frank–Read sources at pre-existing threading dislocation in the epitaxial layer. Generation of such sources is commonly attributed to any points in the layer at which threading dislocations are pinned [6–8]. As a matter of fact these mechanisms describe the following stages of dislocation generation after dislocation nucleation itself. A few papers have been devoted to the study of the initial stages of strain relaxation, i.e. dislocation nucleation [9–11]. Different kinds of heterogeneous sources of dislocation nucleation have been observed: "diamond defects" (faulted dislocation loops with $\boldsymbol{b} = a/6\langle 114\rangle$; 20–200 nm) which act as multiply regenerative sources of 60°-MDs with different $\boldsymbol{b}$ vectors [9]; small vacancy-type dislocation loops which are nucleated at

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Ge-rich platelets (<1.5 nm) localized at the interface [10]; large dislocation loops (50–200 nm) which are formed due to an agglomeration of point defects related to the implantation of near-surface part of the layer with B^+ ions but cannot propagate to form MDs [11]. Accordingly, further investigations of the processes of dislocation nucleation, propagation and multiplication are needed to be continued.

An idea that intrinsic point defects (IPDs) contribute to dislocation nucleation seems to be reasonable. Moreover, an assumption has been put out that the presence of the low-temperature (LT) buffer layer in heterostructure changes the MD nucleation mechanism and/or rate of the dislocation nucleation [3]. In our previous work [12] we have studied the dislocation structure in multilayer $Si_{0.7}Ge_{0.3}$/Si heterostructures with LT-Si and LT-(Si + SiGe) buffer layers. It was found that in these heterostructures the MD generation occurred through mechanisms typical for SiGe/Si heterostructures grown at conventional temperatures (e.g., Perovic–Houghton mechanism [10]), whereas the rate of dislocation nucleation was much higher due to the high vacancy concentration near the interface. However, the dislocation structure formation occurred in these heterostructures during the epitaxial growth; thus, we had no chance to study the initial stages of strain relaxation.

This work focuses on the kinetics of dislocation structure formation in the fully strained $Si_{1-x}Ge_x$/Si heterostructures with LT-Si and LT-SiGe buffer layers during thermal annealing. The main attention is devoted to the MD nucleation at the initial stages of strain relaxation as well as the MD multiplication.

2. Experimental

Heterostructures were grown in a RIBER–SIVA 45 MBE machine. Prior to epitaxial growth, the substrates were cleaned with a standard RCA process followed by annealing at 1035 °C for 15 min in a growth chamber to remove the native oxide. An undoped Si buffer layer was initially grown directly on the substrates at 750 °C. Two types of $Si_{1-x}Ge_x$/Si(0 0 1) heterostructures with Ge content of 0.15 and 0.30 and layer thickness of 200 and 80 nm, respectively, were grown on the LT-Si(400 °C) and LT-SiGe(250 °C) buffer layers with thickness of 50 nm. High-temperature SiGe layers were grown at a substrate temperature of 500 °C. Reference heterostructures were grown without LT layers. 5-nm-thick Si-cap layer was grown on the surface of all heterostructures. Thermal annealing was carried out at 550, 600 and 650 °C for 3–10 min in hydrogen. Structural characterization of the samples was performed by preferential etching/Nomarski microscopy and transmission electron microscopy (TEM). Hereafter the heterostructures studied will be referred as reference, LTSi and LTSiGe heterostructures.

3. Results and discussion

Layer thicknesses of the SiGe alloys were chosen so that being about an order of magnitude greater than the appropriate critical thicknesses which are equal to 19.3 and 8.0 nm for $x = 0.15$ and 0.30, as we calculated using Houghton's approach [13]. Starting from the nominal layer thicknesses, we calculated energy of fully strained interface ($E_\varepsilon \sim \varepsilon^2 h$) [14]. For the reference and LTSi heterostructures, these values are equal to 1.52 J/m^2 ($x = 0.15$) and 2.4 J/m^2 ($x = 0.30$). For the LTSiGe heterostructures, these values are equal to 1.9 J/m^2 ($x = 0.15$) and 3.89 J/m^2 ($x = 0.30$) due to the enhanced thickness of SiGe layer. Chemical etching patterns show that all but two LTSiGe heterostructures have been grown fully strained. TEM examination of cross-sectional samples (Fig. 1) shows that actual layer thicknesses slightly differ from the nominal ones. In as-grown Si/$Si_{0.85}Ge_{0.15}$/LT-$Si_{0.85}Ge_{0.15}$/Si-sub heterostructure, the measured values amount to 7 nm for Si-cap layer, 210 and 80 nm for high-temperature and low-temperature parts of the SiGe layer, respectively. LT-SiGe layer possesses well-pronounced folded contrast in 220 dark-field images.

3.1. Evolution of dislocation structure during thermal annealing

Using post-growth thermal annealing of the heterostructures, we studied different stages of dislocation structure evolution. Annealing conditions and experimental results obtained with the use of preferential chemical etching are summarized in Table 1. We measured linear density of morphological lines (N_L) in cross-hatch revealed on the layer surface and density of dislocation etch pits (N_S) revealed in the near-interface

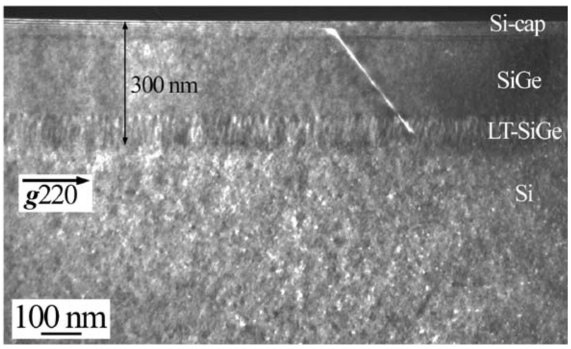

Fig. 1. TEM cross-sectional image of as grown Si/$Si_{0.85}Ge_{0.15}$/LT-$Si_{0.85}Ge_{0.15}$/Si-sub heterostructure.