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Materials Science in Semiconductor Processing 8 (2005) 215–218
MATERIALS SCIENCE IN SEMICONDUCTOR PROCESSING

A comparative analysis of thermal gate oxide on strained Si/relaxed SiGe layer for reliability prediction of strained Si MOSFETs

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Available online 19 October 2004

Abstract

Although the high mobility channel was formed with the strained Si layer on the fully relaxed $Si_{0.8}Ge_{0.2}$ buffer layer, the mobility was severely attenuated with increasing the gate bias due to the degraded interface. The quality of oxide grown on strained Si was found to be worse than that for the unstrained Si in terms of fixed oxide charge, interface state density, oxide traps. Also the degraded oxide quality induces high leakage current, it can be a severe source which gives rise to potential reliability issues and performance degradation in strained Si devices.

PACS: 73.40.Qv; 77.84.Bw; 85.40.−e

Keywords: Strained Si; SiGe; Gate oxide; Reliability; Mobility; MOSFET

1. Introduction

Recently, strained Si channel MOSFETs have attracted much attention due to the enhanced current drivability. It is caused by the increase in the inversion layer carrier mobility. The mobility enhancement in strained Si channel is prominent for moderate effective field at which phonon-related scattering prevails [1–3]. Because the channel mobility and the oxide leakage are very sensitive to the interface and the oxide quality, it is crucial to grow high quality oxide on strained Si. In the present study, we analyze the transport properties of strained channel MOSFETs through the evaluation of mobility parameters. In addition, we performed a comparative study on the electrical properties of thermal gate oxide of the strained Si MOS capacitors and MOSFETs.

2. Experiments

The strained Si wafers, which were produced by SUMCO, have layer stacks composed of a graded SiGe layer (2 μm), a fully relaxed $Si_{0.8}Ge_{0.2}$ buffer layer (1.5 μm), and top strained Si layer (25 nm). A standard CMOS process was used to fabricate the devices and those with conventional substrate were also formed as control device. The capacitance–voltage (C–V), current–voltage (I–V) characteristics were analyzed to study transport properties of the MOSFETs and quality of the

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1369-8001/$ - see front matter © 2004 Published by Elsevier Ltd.
doi:10.1016/j.mssp.2004.09.070

thermal gate oxide and the interface for the strained and the unstrained Si. We adopt the thick gate oxide (~40 Å) for evaluation of the MOS capacitors and the thin one (~15 Å) for the MOSFETs.

3. Results and discussion

First, we extracted the effective inversion carrier mobility which is expressed as $\mu_{eff} = \mu_0/[1 + \theta_1(V_G - V_T) + \theta_2(V_G - V_T)^2]$, where μ_0 and θs are the intrinsic maximum low field mobility and the attenuation factors due to the transverse field, respectively [4]. It is estimated from Fig. 1 that mobilities of electron and hole are increased by 115% and 65%, respectively. This mobility increase gives rise to the current improvement of 78% (NMOSFET) and 21% (PMOSFET) at the same gate overdrive ($|V_G - V_T| = 0.7$ V) as shown in Table 1.

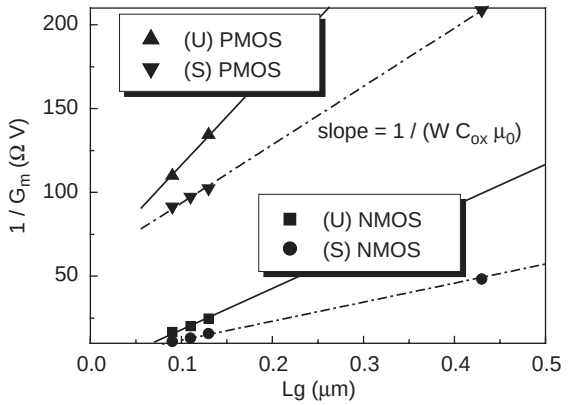

Fig. 1. Plots of $1/G_m$ vs L_g. U and S denote the unstrained Si and the strained Si devices, respectively. G_m is a conductivity parameter defined as $WC_{ox}\mu_0/L_{eff}$. The maximum mobility is proportional to the reciprocal of the slope. The mobility values are given in Table 1.

The mobility parameters are summarized in Table 1, showing that the strained Si devices have higher values of θ_1 and θ_2 as well as μ_0. We point out that, despite the higher mobility at low and moderate vertical field, the strained Si device is deteriorated faster than the unstrained device with increasing gate over-drive. This mobility behavior leads the reduction of Idsat enhancement as the gate over-drive increases (see Figs. 2 and 3). Higher mobility attenuation factors of the strained Si devices are originated from the surface scattering due to both roughness and interface state. Unlike the NMOS, the saturation current of the strained channel PMOS becomes even lower than the unstrained one when the gate bias is high for short channel devices. The estimation of D_{it} for the strained and the unstrained devices shows that the interface state density of strained Si is higher than that of the unstrained Si as given in Table 1. It can be claimed from this result that the degraded oxide interface in the strained Si induces the lower performance for high gate bias. Thus, it is necessary that high gate field should be prohibited in order to obtain better performance in strained Si devices.

The C–V characteristics of NMOS gate oxides (NGox) and PMOS gate oxides (PGox) are shown in Figs. 4 and 5, respectively. The gate oxides on the strained Si are found to have higher accumulation capacitances than the unstrained Si, thus the oxide thickness for strained Si is smaller, as presented in Table 1. It is consistent with the previous report that the growth rate of thermal oxide on strained Si decreases slightly as the strain increases [5]. We also note that the plateau in the C–V plot exists between gate biases of

Table 1
The various device parameters of MOS capacitors and MOSFETs are presented

Device parameters		NMOS		PMOS	
		Unstrained	Strained	Unstrained	Strained
Mobility	μ_0 (cm^2/Vs)	276.7	594.0	124.1	205.1
	θ_1	0.158	0.784	0.929	1.843
	θ_2	0.399	0.451	0.111	0.263
MOSCAP	T_{ox} (Å)	40.0	38.1	42.2	38.9
	V_{FB} (V)	−1.01	−1.14	0.94	0.82
MOSFET ($W/L = 10/5$ μm)	V_T (V)	0.173	0.119	−0.193	−0.211
	SS (mV/dec)	86.857	92.274	79.208	83.496
	DIBL (mV/V)	60	120	140	110
	D_{it} (C/cm^2 eV)	3.13e–12	3.67e–12	2.32e–12	2.99e–12
	ΔI_D (%)		78%		21%

The mobility parameters are extracted from the I–V data using "linearization method" (Ref. [4]). Here θ_1 and θ_2 represent attenuation factors due to transverse field. The mobility parameters and MOSFET parameters are extracted from the devices with the thin gate oxide (~15Å). The interface state density (D_{it}) is extracted from the subthreshold characteristics.