Available online at www.sciencedirect.com
SCIENCE DIRECT®
Materials Science in Semiconductor Processing 8 (2005) 225–230
MATERIALS SCIENCE IN SEMICONDUCTOR PROCESSING

Application of plasma oxidation to strained-Si/SiGe MOSFET

Mika Nishisaka*, Tanemasa Asano

Center for Microelectronic Systems, Kyushu Institute of Technology, 680-4 Kawazu, Iizuka, Fukuoka 820-8502, Japan

Available online 13 October 2004

Abstract

We have applied microwave-plasma oxidation to the gate oxide formation of strained-Si metal-oxide-semiconductor field-effect-transistor (MOSFET). Change in surface morphology of plasma oxidized strained-Si/SiGe is studied using an atomic force microscope (AFM) and compared with thermal oxidation. The AFM observation is carried out before and after oxidation in an identical area of a single sample. Plasma oxidation at 400 °C which proceeds under diffusion-limited condition suppressed nonuniform oxide growth caused by cross-hatch related surface morphology and is able to form gate oxide on strained-Si/SiGe without increase in surface roughness. Strained-Si n-channel MOSFETs on 15%-Ge content wafer were fabricated and the transconductance was enhanced by 70% compared with unstrained Si devices.

PACS: 81.65.Mq; 81.05.Cy; 73.40.Qv; 68.35.Ct

Keywords: Strained-Si; Plasma oxidation; MOSFET; Surface roughness

1. Introduction

Strained-Si metal-oxide-semiconductor field-effect-transistors (MOSFETs) have attracted much attention because of their improved mobility and current drive capability [1,2]. The 4.2% lattice mismatch between Si and Ge gives rise to strained-Si when Si is epitaxially grown on relaxed SiGe. In order to prevent strain relaxation and interdiffusion at the strained-Si/SiGe interface, however, long heat treatment at temperatures over 850 °C should be avoided. One of the key considerations in fabricating strained-Si devices is oxidation. We have found that surface roughness increases when thermal oxidation is applied to strained-Si/SiGe to form gate oxide [3]. The increased roughness can cause a decrease in channel carrier mobility. Spatial non-uniformity in strain in the strained-Si film, which is related to the cross-hatch, is a possible cause for the increased roughness because strain enhanced oxidation takes place [3]. Therefore, in order to minimize the increase in surface roughness, oxidation under diffusion-limited condition should be effective. Plasma oxidation at low temperature proceeds under diffusion-limited condition from the early stage of the oxide growth [4,5].

In this work, we apply microwave-plasma oxidation to the gate oxide formation of strained-Si MOSFET. We show that mobility enhancement predicted by theory is achieved using plasma oxidation. Effects of hydrogen plasma treatment are also reported.

2. Experimental

The strained-Si samples used in this study were grown by chemical vapor deposition (CVD). A 2-μm-thick

*Corresponding author. Tel.: +81 948 29 7589; fax: +81 948 29 7586.
E-mail address: mika@cms.kyutech.ac.jp (M. Nishisaka).

1369-8001/$ - see front matter © 2004 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mssp.2004.09.051

graded SiGe layer was first grown on Si (1 0 0) followed by the growth of 1-μm-thick $Si_{1-x}Ge_x$ ($x = 0.15$, 0.3) layer and the growth of 20-nm-thick strained-Si layer.

The gate oxide films were grown using a 2.45 GHz microwave plasma. No gas other than pure O_2 was supplied . The pressure and the incident microwave power were 0.5 Pa and 100 W, respectively. The plasma oxidation at 400 °C using our equipment followed the parabolic law for oxide thicker than 2.5 nm, indicated that the oxidation proceeded under the diffusion-limited condition. The oxidation was carried out at 400 °C for 3 h. This condition grows 5 nm-thick oxide on Si-control wafer. For comparison, thermal dry oxidation at 800 °C was performed.

In order to observe the same point on a sample with atomic force microscope (AFM) (hereafter, we designate as identical-point AFM) to trace the change in surface morphology, a mesa pattern was defined on the surface of the strained-$Si/Si_{0.7}Ge_{0.3}$ wafers using reactive ion etching (RIE) with CF_4 gas. Each mesa has the diameter of 20 μm and the height of 200 nm. After RCA cleaning, oxidation was performed. The first AFM observation was carried out prior to oxidation. After oxidation, AFM observation of the same area as in the first observation was carried out by utilizing the mesa pattern for the point search. For some samples, removal of the oxide and re-oxidation were carried out, followed by observation by identical-point AFM. In order to avoid the influence of strain relaxation which may take place near the edge of the mesa, AFM observations were carried out near the center of the mesa circle.

N-channel strained-$Si/Si_{0.85}Ge_{0.15}$ MOSFETs were fabricated. The maximum process temperature was set at 800 °C to prevent interdiffusion at the strained-Si/SiGe. An oxide film deposited by PECVD was used for device isolation. Gate oxide was formed by plasma oxidation. Samples, for which the gate oxide was formed by thermal oxidation at 800 °C for 3 h, were also prepared for reference. A 300-nm-thick polycrystalline Si (poly-Si) film was deposited as the gate electrode by low-pressure CVD (LPCVD) at 600 °C. After gate patterning, self-aligned source/drain implantation was carried out using P^+-ions (55 keV, 2×10^{15} cm^{-2}) followed by annealing in N_2 at 800 °C for 20 min. A conventional Si MOSFETs were also fabricated on 2–6.5 Ω cm *p*-type wafers with the same sequence.

3. Results

3.1. Surface morphology

Figs. 1(a) and (b) show cross-sectional transmission electron microscopy (TEM) images of the gate oxide grown at 800 °C by thermal oxidation and 400 °C by plasma oxidation, respectively, at the strained-Si/

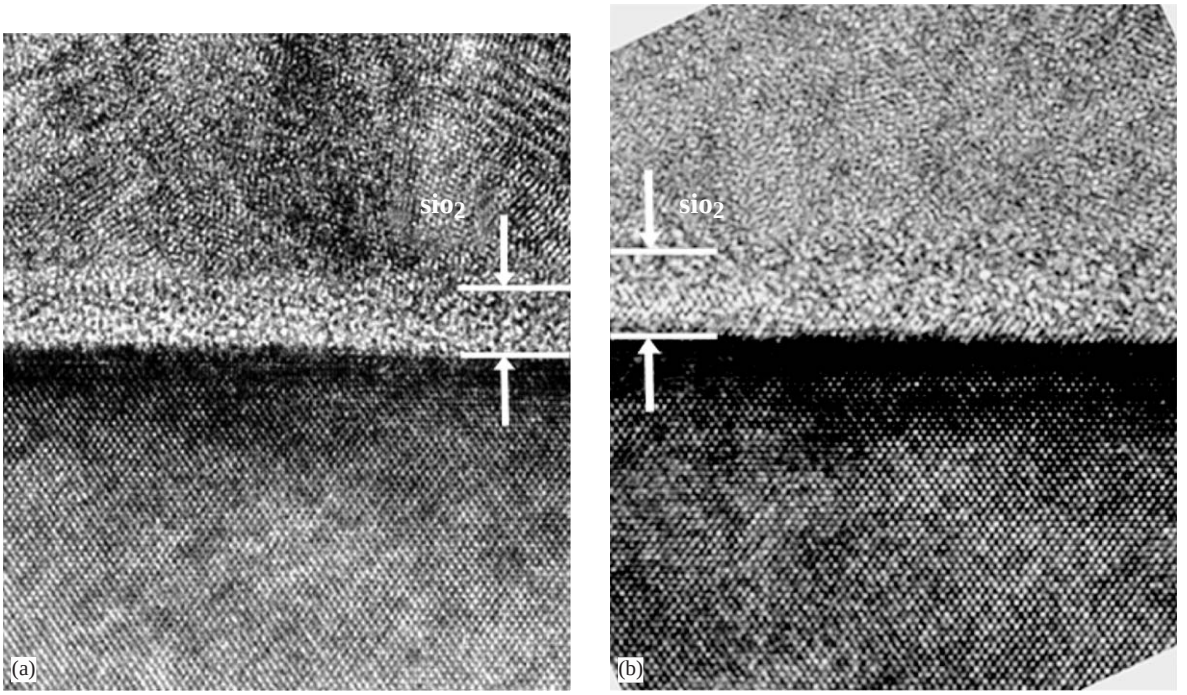

Fig. 1. High-resolution TEM images of the Si/SiO_2 interface in MOS gate structures: (a) thermal oxide grown at 800 °C and (b) plasma oxide grown at 400 °C.