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Trends, demands and challenges in TCAD

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Abstract

Currently, TCAD is most heavily used in the device research and process integration phases of a technology life cycle. However, a major trend visible in the industry is the demand to apply TCAD tools far beyond the integration phase into manufacturing and yield optimization. Short IC product lifetimes make fast yield ramp-up critical for being profitable and TCAD tools build a bridge between IC design and manufacturing. Another major trend is to use TCAD to evaluate layout dependent stress variations and account for these variations in the design flow of standard cells, libraries and custom ICs. This article gives an overview of those trends and addresses resulting challenges for TCAD models and tools.

Keywords: TCAD; ACP; Semiconductor technology

1. Introduction

When looking at trends, demands and challenges in TCAD one certainly needs to look at the semiconductor technology trends itself first. And since this article cannot cover the complete application space of TCAD, it will focus on application segments which have not been addressed often in the past: TCAD for IC design and manufacturing.

The most challenging issue in the context of IC design and manufacturing is product yield because the main causes for yield loss have changed over the years. Since several semiconductor technology generations, yield is not dominated by random defects anymore (Fig. 1). Instead, process variations and systematic defects are largely dominating yield at current most advanced technology nodes [1]. The sources of these process variations and systematic defects must be identified and controlled in order to minimize yield loss. Since TCAD virtually reveals the view *into* silicon, it is a powerful tool to identify root causes for yield loss. Moreover, TCAD simulations can accurately predict the impact of process variations on device performance and can therefore be used to reduce yield loss caused by such fluctuations. Both applications will be discussed in detail below and examples will illustrate the use of TCAD for design and manufacturing. The potential benefit TCAD gives in this application field will probably be one of the main driving forces behind the development and calibration of more accurate simulation models.

2. TCAD for manufacturing

So far TCAD is mainly used during the technology development phases from device research to process integration and only very little after a technology has been transferred to production. One reason is certainly that numerical simulations are by far too slow to give timely answers to many questions arising during a manufacturing process. In addition, the usage of TCAD tools requires a high level of specific know-how which represents a certain barrier for production engineers to use such tools. These problems can be largely reduced by using response surface models of analytical or numerical nature, directly linking process parameters with device parameters. Such compact models, in the following called Process Compact Models (PCMs), are derived from data generated by systematic process- and device simulations. They are easy to use and give results in milliseconds while numerical simulations need CPU times on the order of hours.

The generation of a PCM starts with a Design-of-Experiment (DOE) based on process variations taken from manufacturing equipment (Fig. 2). Depending on the complexity, several hundred to several thousand TCAD simulations are required to fully characterize the impact of such process variations on device performance. The extraction of PCMs from such data is an optimization task similar to that known from device compact models. The compact model parameters are optimized until the

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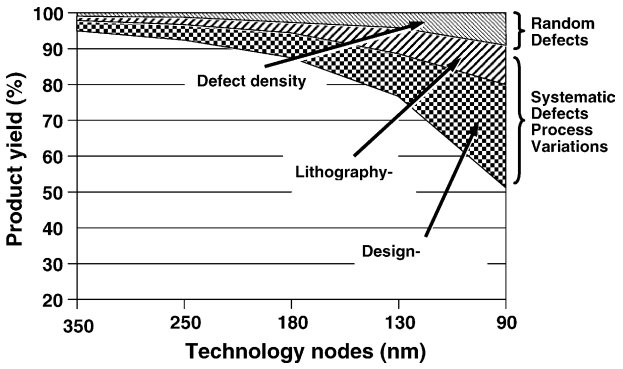

Fig. 1. Yield loss caused by random defects, lithography and design for technology nodes from 350 to 90 nm. With decreasing feature size lithography based and design based yield loss dominate overall product yield and both mechanisms become highly sensitive to process variations.

error between the compact model and the TCAD generated data reaches its minimum. The accuracy penalty for going from the complete set of numerical data to compact models should not exceed a few percent.

The biggest challenge in generating valuable PCMs is the calibration of the underlying process- and device simulations. The better the numerical simulations are calibrated and the better the simulation models reproduce process-device sensitivities, the more accurate the compact models are. In the future, this will probably be one of the main driving forces for advanced calibration of process- and device simulators and for the continued development of physical simulation models. For a standard 90 nm CMOS process the required accuracy level is already achievable with today's simulation tools. Fig. 3 shows a comparison between SIMS measurements and simulation results of an As S/D extension profile and B halo implantation profile at the end of the process flow [2]. Electrical comparison for the same technology at three different halo implantation doses is shown in Figs. 4 and 5. The overall accuracy of simulated electrical

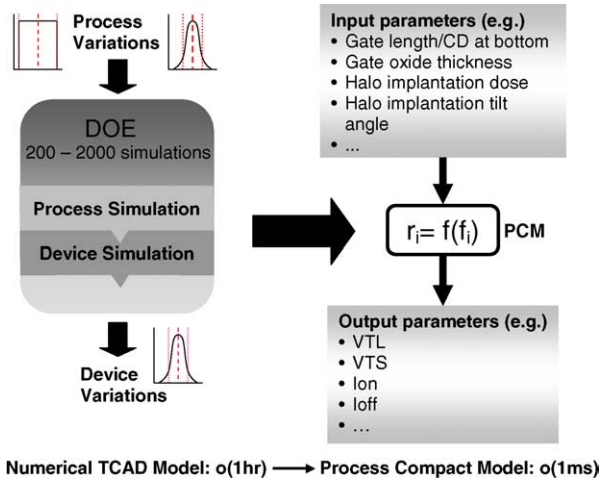

Fig. 2. Process Compact Models (PCMs) are derived from Design-of-Experiments (DOE) where statistical process variations are taken as the input for process- and device simulations. The PCMs extracted from DOE results, directly link process input parameters to device output parameters and can be evaluated in milliseconds.

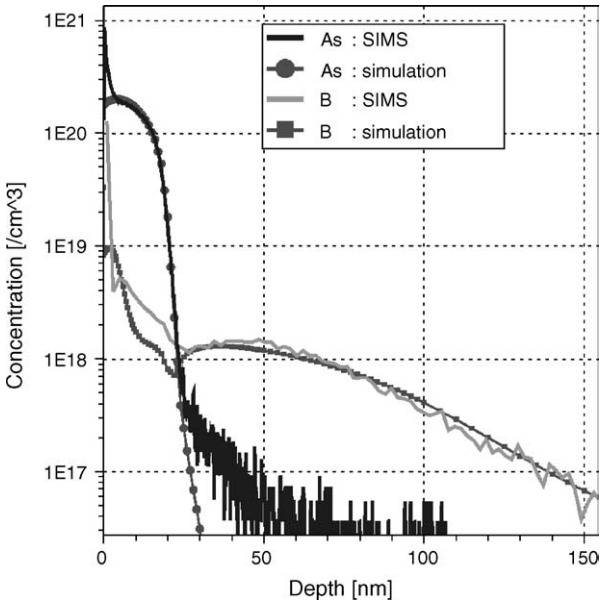

Fig. 3. Comparison between SIMS measurements and simulation results of the arsenic S/D extension and boron halo implantation profile of a 90 nm NMOS transistor.

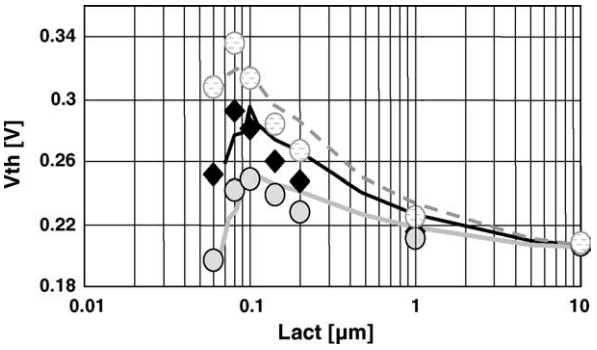

Fig. 4. Threshold voltage vs. effective gate length of NMOS transistors at high drain bias for three different halo doses fabricated with a 90 nm technology (symbols: simulation results, lines: median of experimental results).

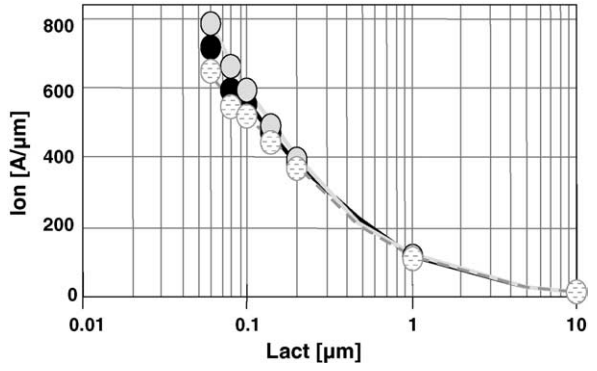

Fig. 5. Drain current vs. effective gate length of NMOS transistors at high drain bias for three different halo doses fabricated with a 90 nm technology (symbols: simulation results, lines: median of experimental results).