

Suppression of boron interstitial clusters in SOI using vacancy engineering

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Abstract

As CMOS devices scale into the 45 nm process window, the requirements for the individual devices become even more stringent, with levels of activation well above solid solubility with minimal dopant diffusion.

Boron interstitial clusters (BICs) are known to hinder the activation of typical boron implants reducing the level of activation even below solid solubility. This paper reports on an optimised vacancy engineering technique to reduce the interstitial population, which would normally occur after ion implantation. Hence, the BIC formation is suppressed creating a highly active layer, which remains active over a 700–1000 °C temperature window. Using this technique, it has been estimated that at 700 °C the level of activation may be around $5 \times 10^{20} \text{ cm}^{-3}$ rivaling techniques such pre-amorphisation combined with solid phase epitaxy re-growth.

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1. Introduction

It is well known that forming low resistive p-type layers is foreseen as a challenge for future CMOS devices. As the source/drain regions are scaled into the 45 nm process window the device requirements become increasingly more stringent with dopant electrical activation needed well above solid solubility, with minimal dopant movement. As boron is the most popular choice of dopant for the PMOS device these requirements are difficult to achieve due to process related phenomena such as transient enhanced diffusion (TED). Another problem associated with boron doping is related to the enhanced clustering driven by the non-equilibrium saturation of silicon interstitials remaining from the ion implantation process. The boron interstitial clusters (BICs) thus formed are electrically inactive, immobile and appear at concentrations well below solid solubility [1].

The conventional method of overcoming these problems is to use a pre-amorphisation implant (PAI) coupled with solid phase

epitaxial re-growth (SPER). However, this leads to end-of-range defect formation with concomitant source/drain deactivation during subsequent thermal steps [2], as well as the presence of defects in device channel regions. This paper investigates using optimised vacancy engineering as a potential solution to such problems.

Vacancy engineering is a technique, which typically has used a high energy silicon co-implant (500 keV–MeV) before the doping implant. The method relies on the underlying principle that momentum transfer from the high energy ions to the host atoms causes the Frenkel pair (interstitial and vacancy) populations to become spatially separated [3]. During interstitial–vacancy recombination (dynamically or during thermal processing) a net increase in vacancy defects occurs in the near surface region with a corresponding net increase in interstitials around the projected range of the Si implant and beyond. It is this vacancy engineered surface region, which is used to enhance the activation [4,5] and reduce the diffusion [6,7] of the low energy boron doping implant.

Previously, we have shown that it is possible to optimise vacancy engineering in terms of the ion energy and dose when using a SOI substrate, to make the technique more applicable to industry [8]. This is due to the fact that silicon interstitials recoiled through the buried oxide (BOX) are unable to diffuse

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back to recombine with the vacancies in the surface silicon layer [9]. Therefore, if a thin SOI structure is used, a medium to low silicon ion energy can be used.

In this paper, we report on improved low temperature activation with minimal diffusion of a 500 eV B implant using a medium energy (160 keV) Si vacancy engineering implant.

2. Experimental

UNIBOND standard p-type 55 nm/145 nm/Bulk SOI wafers were used. A silicon ion energy of 160 keV was chosen in order to position the majority of the interstitial damage distribution beneath the BOX, with a significant portion actually residing in the BOX, so that the minimum ion energy could be used for this specification of SOI. Three silicon doses were chosen, 4×10^{14} , 8×10^{14} and $1.1 \times 10^{15} \text{ cm}^{-2}$. The amount of damage to the substrate was determined by transmission electron microscopy (TEM).

After the vacancy engineering implants an ultra-low energy boron (500 eV) implant was performed to a dose of 10^{15} cm^{-2} at the same implant geometry as the Si implants. One SOI wafer was implanted with boron only as a reference sample.

All anneals were performed in a Process Products Corp., 18 lamp, rapid thermal annealer under a nitrogen ambient. A 10 s isochronal annealing regime was applied from 700 to 1000 °C.

Hall effect and SIMS measurements were performed to determine the effects on the electrical activation and diffusion, respectively. The Hall scattering factor for this study has been assumed to be unity.

3. Results and discussion

The effect of the 160 keV silicon co-implant can be distinctly seen in Fig. 1 where the sheet resistance (R_s) is plotted as a function of silicon co-implant dose at 900 °C. The reference boron sample with no silicon co-implant is represented at the zero point on the x-axis. It is clearly seen that by introducing an excess of vacancies a lower resistance p-type layer is formed.

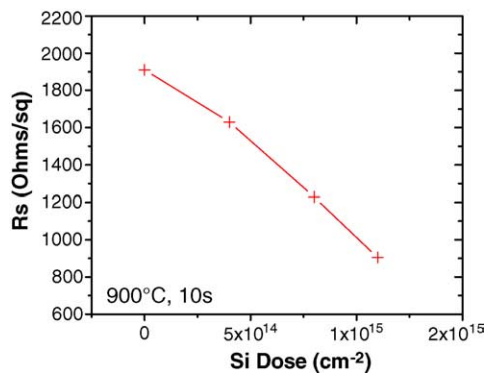


Fig. 1. R_s measurements of a boron implant with and without a silicon co-implant, plotted as a function of silicon co-implant dose at 900 °C. The boron implant with no Si co-implant is represented on the x-axis at 0 for comparison.

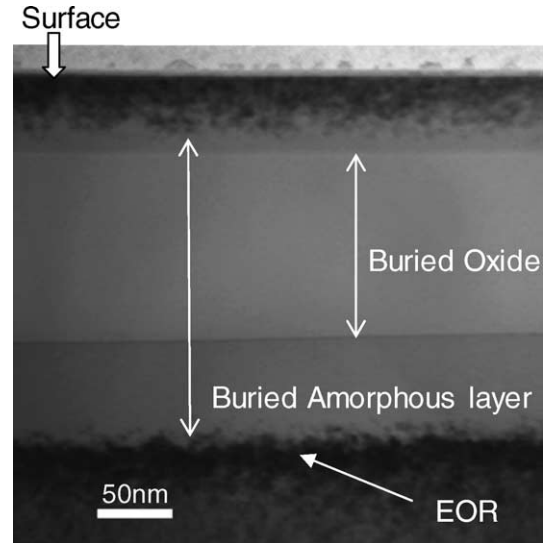


Fig. 2. TEM analysis shows the effect of a $1.1 \times 10^{15} \text{ cm}^{-2}$ silicon co-implant in SOI, after implantation.

As the silicon dose is increased it is assumed the concentration of vacancies increases and this has a larger effect on the boron implant. One can see that in the $1.1 \times 10^{15} \text{ cm}^{-2}$ Si case the improvement in R_s is over a factor of two compared to the no co-implant case.

In principle, the improvements in boron activation should continue to increase as a function of the concentration of implanted vacancies. However, this is limited in practice by the fact that very large silicon doses will completely amorphise the surface layer, eradicating the generated vacancies. It is known that implanting at elevated temperatures [10] can eliminate amorphisation but the impact of this on the surface vacancy rich region is unknown.

Another approach is to increase the silicon dose up to and just beyond the amorphisation threshold to form a buried amorphous layer, keeping the surface region crystalline and highly vacancy rich. The SPE re-growth of a buried amorphous layer has been studied by El-Ghor et al. [11], showing a difference in re-growth velocities of the two interfaces on either side of the amorphous region. The top interface with the vacancy rich region re-grew more slowly than the bottom interface with the deeper interstitial-rich region. This was attributed to the different type of defects surrounding the two interfaces.

For the remaining part of this paper the investigation will be focused on the highest dose ($1.1 \times 10^{15} \text{ cm}^{-2}$) silicon co-implant, which has been specifically designed to create a buried amorphous layer and a very highly vacancy rich near surface layer. X-TEM analysis was performed to check the level of damage created by this silicon implant. This can be seen in Fig. 2, showing the damage created in a SOI structure from the silicon co-implant. One can see that a buried amorphous layer extends from around 235 nm towards the surface for 195 nm, leaving a 40 nm surface region in which the boron is implanted. This has two main advantages: firstly, the EOR damage is located beneath the BOX isolating it completely from the top layer. Secondly, the surface layer is extremely vacancy rich but contains enough

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