

Leakage current and deep levels in CoSi₂ silicided junctions

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Abstract

In this work the leakage current of junctions with a self-aligned cobalt silicide is studied. It is shown that junctions with a self-aligned CoSi₂ layer show a leakage current excess which is strongly reduced by increasing the PAI energy. This indicates that the observed leakage current excess is related to the CoSi₂ formation conditions. The mechanism responsible for the leakage of CoSi₂ junctions is investigated by current versus temperature measurements and by deep level transient spectroscopy. In addition, the role of the mechanical stress is investigated by comparing different isolation structures and by numerical stress calculations.

It is concluded that the shallow trench isolation (STI) induced stress and the cobalt silicide formation concur to produce a junction leakage current increase by creating a deep level in silicon located close to midgap. This level can possibly identified with a level ascribed to a point defect excess.

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1. Introduction

The formation of a cobalt silicide over the source and drain junctions is widely used in device processing to reduce the resistance of the source and drain regions. It is reported that the CoSi₂ formation is associated with a leakage of the source and drain junctions. This phenomenon is ascribed to a localized leakage due to cobalt silicide spikes [1], or to an effect of the mechanical stress induced by the silicide layer [2]. In this work, we show that the junction leakage current can also be affected by the formation process of the junction self-aligned silicide because of the introduction of deep levels in the space charge region of the junction.

2. Experimental details

2.1. Sample preparation

Both n⁺/p-well and p⁺/n-well junctions were studied. The junction active area was defined by the shallow trench isolation (STI), n-type and p-type areas were obtained by implantation, and in these areas, the n⁺–p and p⁺–n junctions were formed by arsenic and boron implantations, respectively. After a recrystal-

lization annealing (furnace plus RTP), the wafers received a pre-amorphization implantation (PAI) with arsenic (implantation energy in the range 20–40 keV). For comparison purposes, some wafers skipped this implantation. A cobalt layer was deposited and CoSi₂ was formed by a two-step RTP.

In order to investigate how mechanical stress affects our results, in some samples the trench depth was reduced by about 10%, as mechanical stress was found to increase significantly with increasing the trench depth. Finally, in some samples the CoSi₂ layer was replaced by a TiSi₂ layer.

In order to investigate geometry-related effects, structures with different geometries were studied, namely area diodes (rectangles with 0.13 mm² area and 3.42 mm perimeter) and perimeter diodes (narrow stripe diodes with a total area of 0.065 mm² and a perimeter of 40.8 cm).

2.2. Experimental techniques

The junctions were electrically tested at 8 V reverse bias. After testing, the current–voltage characteristics of the junctions were measured as a function of temperature and a deep level transient spectroscopy (DLTS) analysis was carried out. A DLS-83D instrument by Semilab was used. In this instrument lock-in integration is used for averaging capacitance transients and temperature can be scanned from about 30–300 K. Alternatively, constant temperature spectra can be obtained as a function of the frequency of excitation pulses [3] in the range 0.5–2 kHz.

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Both methods were used in this work. The differential DLTS method [4,5] was used in order to reduce the edge effect. In this method two filling pulses are applied, a first pulse in the beginning of the integrating period and a second pulse a half period later. In the lock-in integration, the integral of the capacitance transient caused by the first pulse is taken with positive sign, and the integral of the capacitance transient caused by the second pulse is taken with negative sign. The edge effect contribution is approximately independent of voltage, so this contribution is cancelled out by this procedure, resulting in a more precise concentration measurement. The differential DLTS technique also allows the deep level profile to be obtained [5]. In our measurements, the junctions were reverse biased at -5 V, and $10\text{ }\mu\text{s}$ filling pulses with 4.5 and 0.5 V amplitudes were applied during each integrating period.

3. Experimental results

3.1. Reverse current measurements

The leakage currents of both n^+/p and p^+/n junctions were found to increase with decreasing the PAI energy and to be

maximum if the silicide is formed with no pre-amorphization (see Fig. 1). This effect is most evident in n^+-p structures, but it is also present in p^+-n structures. As a comparison, Fig. 2 shows the leakage current distributions with 40 keV PAI and with no PAI, when the trench depth is decreased by 10% . By comparing these data with those in Fig. 1, the same effect of the pre-amorphization on the leakage current is observed, but in this case in the absence of a pre-amorphization the leakage current increase is less pronounced.

In order to investigate the reason of this leakage current increase the junction reverse current I was measured as a function of temperature T . Low leakage and high leakage diodes obtained by 40 keV PAI energy were chosen for these measurements. Fig. 3 reports $I/T^{3/2}$ as a function of $1/T$ for area and perimeter diodes and shows that the reverse current depends on temperature as $I \propto T^{3/2} \exp((E_g/2 + \Delta E)/kT)$, where E_g is the silicon energy gap and ΔE is the energy difference between the level responsible for generation and midgap. From the plot in Fig. 3, $0 \leq \Delta E \leq 0.05\text{ eV}$, so Fig. 3 show that both in area and in perimeter diodes the reverse current is dominated over the whole measurement range by a generation contribution due to a level located close to midgap. High leakage and low leakage

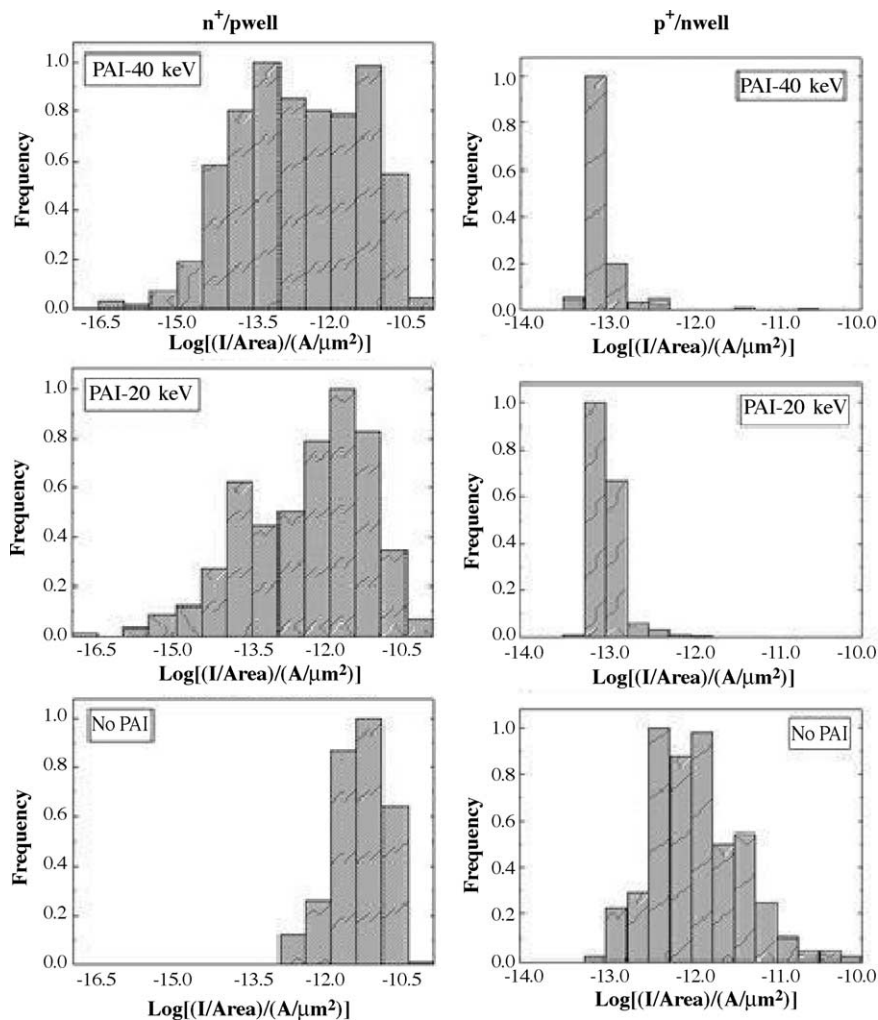


Fig. 1. Reverse current distributions of n^+-p and p^+-n junctions with two different PAI energies and with no pre-amorphization.

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