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Characterization of a high-density plasma immersion ion implanter with scaleable ECR large-area plasma source

Yuri Glukhoy[a,1], Mahmud Rahman[b,*], Gotze Popov[a,1], Alexander Usenko[c,2], Hans J. Walitzki[d,3]

[a]*American Advanced Ion Beam, Inc., 440 Arguello Blvd, #1, San Francisco, CA 94118, USA*
[b]*Department of Electrical Engineering, Electron Devices Laboratory, Santa Clara University, 500 El Camino Real, Santa Clara, CA 95053 0583, USA*
[c]*Silicon Wafer Technologies, Inc., 240 King Blvd., Newark, NJ 07102, USA*
[d]*Isonics Corporation, 12514 NE 95th Street C-110, Vancouver, WA 98682, USA*

Abstract

A key issue for future high-performance CMOS techniques is the fabrication of 12 in. or larger silicon-on-insulator (SOI) wafers with thickness of the top silicon layer under 25 nm. The electron cyclotron resonance (ECR) plasma ion immersion implanters (ECR-PIII) are viable candidates to realize the above.

We designed an ECR-PIII in which we integrated the new concept of a large-area plasma source. This new plasma source is an array of elementary ECR plasma sources created by an assembly of *m* linear microwave sources. Each linear microwave source has *n* radiating elements ($n > m$) and includes a system of permanent magnets that create magnetic induction for ECR to occur in the processing chamber. An array of 90 elementary ECR plasma sources generate highly homogeneous dense plasma with dimensions permitting processing of 12-in. wafers.

Since hydrogen implantation requiring high dose often results in blistering of the wafer surface, a new Smart-Cut™-like technology has been suggested (US Patent 6,352,909) where the one-step hydrogen implantation is replaced by a two-step process. The designed ECR-PIII can offer substantial advantage in providing the high yield of protons used for the micro-bubble formation in the two-step process.

Keywords: Electron cyclotron resonance (ECR) plasmas; Plasma immersion ion implantation (PIII); Microwave; Hydrogen; Silicon; Silicon-on-insulator (SOI)

1. Introduction

We have designed an electron cyclotron resonance (ECR) plasma ion immersion implanter (ECR-PIII) particularly suitable for fabrication of 12-in. bonded thin-layer silicon-on-insulator (SOI) wafers. As the semiconductor industry moves from 0.13 μm to <50 nm and beyond line width, thin-layer SOI is expected to be the technology of choice for high-performance CMOS systems. The ECR-PIIIs are anticipated to replace the standard ion implanters for fabrication of 12 in. and larger thin-layer SOI wafers.

The most advanced methods for manufacturing bonded SOI wafers are the layer transfer methods. Smart-Cut™ [1] was the first layer transfer method described in the literature.

It gives high-quality top layer in a final SOI wafer. However, the Smart-Cut™ is not well suited for making SOI wafers with a top layer thinner than 100 nm. Recently, Usenko et al. [2] suggested an improved layer transfer method which allows manufacturing of SOI wafers with thinner top layers required for next-generation chips.

The layer transfer method consists of the following steps:

- forming a fragile plane layer inside of a Si wafer called “donor wafer”
- forming a silicon dioxide layer on top of another Si wafer, called “handle wafer”

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* Corresponding author. Tel.: +1 408 554 4175; fax: +1 408 554 5474.
E-mail addresses: Glukhoy1@aol.com (Y. Glukhoy), mrahman@scu.edu (M. Rahman), Gotzepopov@aol.com (G. Popov), http://www.si-sandwich.com, usenko@si-sandwich.com (A. Usenko), hwalitzki@isonics.com (H. Walitzki).
[1] Tel./fax: +1 415 751 7666.
[2] Tel.: +1 973 297 1410; fax: +1 973 297 1125.
[3] Tel.: +1 360 885 9310x205; fax: +1 360 885 9311.

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- bonding the top side of the donor wafer to the top side of the handle wafer, “sandwiching” the silicon dioxide layer in between
- separation of the donor wafer along the fragile plane.

In this way, a bonded SOI wafer consists of a handle wafer with buried oxide layer and the top layer that has been separated from the donor wafer.

The separation techniques depend on the how the fragile plane layer is formed. In the Smart-Cut™ method, the fragile layer is formed by hydrogen ion implantation at high ion dose such as $5\times10^{16}/\text{cm}^2$ and at an ion dose rate less than $10^{15}/\text{cm}^2$ s. The depth to which the hydrogen ions penetrate into silicon determines the inherent thickness of the transferred layer. For typical ion implantation, energies between 30 and 100 keV, the corresponding depth is 0.3–1 μm.

Implantation at low energy raises several problems. When a high-energy ion reaches the target Si, it dissipates its energy mostly because of interactions with the electronic subsystem of the Si crystal. The energy of the penetrating ion gradually decreases as its energy is transferred mostly to the target’s electrons. When the ion energy drops to $\cong 10$ keV, the ion produces mostly atomic displacements. Ion implantation at low energy, e.g., 10 keV and less, produces effective atomic displacements also at the surface of the target resulting in the formation of a damaged layer that is not buried under the target’s surface. This damaged surface has an increased roughness and cannot be bounded to another (handle) wafer [3].

The process for ultra-thin SOI fabrication proposed by Usenko et al. consists of the following steps (also see Usenko, US Patent 6,352,909 B1 [4]):

- forming a buried trap layer for hydrogen in the donor wafer substrate
- nucleation of hydrogen platelets in the above buried trap layer by hydrogenation at a temperature less than 250 °C
- growing hydrogen platelets in the buried trap layer by hydrogenation at temperatures in the range of 250–400 °C, thus forming a buried fragile layer in the donor wafer
- forming a silicon dioxide layer on the top surface of the handle wafer
- activating the top surfaces of donor and handle wafers
- forming a temporary wafer assembly by making initial contact of the activated surfaces of the donor and handle wafers
- separating the above wafer assembly into two wafers by cleaving the assembly at the buried fragile layer.

The buried trap layer for hydrogen is created by ion implantation. The ions used for such implantation could be either those that do not have electrical activity in the Si crystal, e.g., oxygen ions, or the same ions as the substrate, i.e., Si, or noble gas ions that do not chemically interact with silicon. Hydrogen is delivered to the buried trap layer from a hydrogen plasma, and this defect layer serves as an infinite capacity trap for hydrogen.

The ECR-PIII can be used for manufacturing SOI wafers by the Smart-Cut™ method as well as thin-layer SOI wafers by the Usenko’s process. For the Usenko process, ECR-PIII can be used for both noble gas ion implantation and hydrogenation at ion energies of approximately 20 keV and at the temperatures mentioned above.

The ECR-PIII consists of the following systems:

- processing chamber, which includes an assembly of *m* linear microwave sources used to create a highly homogeneous dense plasma
- high-vacuum system
- gas delivery system
- wafer transfer and positioning system
- microwave generators and HV power supplies for the generators
- pulsed HV generator for application of short negative HV pulses at the implantation target
- a computer controller and PLC that ensure the proper function of all subsystems.

2. The scalable plasma source

Microwaves can generate and sustain plasma at low pressures. In the absence of a magnetic field, the plasma density, n, is limited by the frequency of the microwave, ω, according to the following relationship:

$$n \leq n_\text{c} = \omega^2 \varepsilon_\text{o} m / e^2,$$

where n_c is the critical plasma density, ε_o is the dielectric constant in vacuum, and m and e are the mass and the charge of an electron, respectively.

When a steady magnetic field B is now applied to the microwave plasma, an electron cyclotron resonance (ECR) occurs. This is a resonance between the applied microwave frequency ω and the cyclotron frequency $\omega_\text{c}=eB/m$. At ECR conditions, the electrons rotate along the magnetic field lines in phase with the right-hand circularly polarized microwaves and obtain sufficient energy to ionize the ambient gas. The injection of microwave along the magnetic field allows it to propagate in a dense plasma and create plasma densities $>n_\text{c}$.

A standard ECR plasma source includes a cylindrical chamber. The microwave power is applied to the chamber via a low-loss dielectric window positioned perpendicular to the chamber axis. Magnetic field coils generate nonuniform axial magnetic field $B(z)$ within the chamber, and its magnetic induction can achieve the ECR condition in one or more points on the axis. In such a configuration, it is almost impossible to obtain a homogeneous plasma with dimensions that permit processing of 300-mm wafers. Our approach to this problem is based on the new concept of