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Pentacene-based thin film transistors used to drive a twist-nematic liquid crystal display

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Abstract

The study addresses the factors of influence on the active matrix display that is driven by pentacene-based organic thin-film transistors (TFTs). The atmosphere and humidity conditions were found to seriously affect the performance of organic TFTs. An appropriate encapsulation layer was added to protect the organic TFTs from external damage. Organic TFTs reliability, the illumination effect and device uniformity, were also considered in the context of display application. Finally, a monochrome 3 inch 64 × 128 active-matrix twist-nematic liquid crystal display (LCD) was fabricated. The display is capable of showing video images with a refresh rate of 20 Hz. Obtained results reveal the potential of organic TFTs for active-matrix LCD technology.

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1. Introduction

Organic thin film transistors (OTFTs) have attracted much attention over the last decade. They can be used in a wide range of electronic devices such as displays, radio frequency identification tags [1], smart cards, microelectronics [2–6] or sensors [7]. Among various organic semiconductors, pentacene, a fused ring polycyclic aromatic hydrocarbon, has exhibited a high field-effect mobility of above 1.0 cm^2/Vs and is considered to be the preferred candidate for replacing amorphous silicon thin film transistors (TFTs) [8–11]. Pentacene, a small-molecule organic compound, can be processed by thermal evaporation or vapor deposition. Other organic semiconductors, the long chain polymers, such as regioregular poly(3-hexylthiophene) [12–14] and poly(9,9′-dioctyfluorene-*co*-2,2′-bi-thiophene) [15,16], have less favorable characteristics as compared to pentacene. However, the latter can be fabricated in solution processes, such as spin coating, ink-jet printing [17] or contact printing. Consequently, long chain polymers can be fabricated at lower cost by utilizing a roll-to-roll process — resulting in expenditures equal to 10% of the cost of fabricating traditional TFTs. OTFTs can be fabricated at low temperature and are highly compatible with a flexible/plastic substrate. Inherent features of OTFTs make the technology a promising candidate for the next generation of TFTs.

In active-matrix liquid crystal displays (AMLCDs), for instance, OTFTs allow the use of inexpensive, lightweight mechanically rugged plastic substrates as an alternative to glass. Prototype AMLCDs with all pixels driven by pentacene transistors [18] have recently been demonstrated. A polymer pixel engine has also been developed [19,20],

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indicating the potential for application of organic transistor technology in displays. However, high operating voltage and photosensitivity of OTFTs restrict their use in regular display types. Thus, research on the application of OTFTs to drive AMLCDs, focuses on reflective displays, such as the polymer dispersed liquid crystal or electronic-ink displays [21]. These types of displays are suitable for operation at a high voltage.

This work studies the factors affecting the driving of a twist-nematic liquid crystal (TNLC) with a backlight system by pentacene transistors. Electronic stability of pentacene transistors is always a significant factor of consideration, regardless of application. The study of environmental factors, including moisture and illumination sensitivity of pentacene transistors is presented below. An extra passivation layer was added on to the pentacene transistors to isolate them from the atmosphere and prevent damage from the subsequent TNLC process. The gate bias stress and device uniformity were also studied. A 3 inch transparent active matrix TNLC display with 64×128 pixels was fabricated. The display is capable of displaying a black and white image with a contrast ratio similar to that of a paper. Furthermore, it can easily be fabricated into a color display through application of color filters.

2. Experimental details

This study employs the standard inverted-coplanar thin-film transistor structure with a bottom-contact configuration: the organic semiconductor is deposited onto the gate insulator, the prefabricated source and the drain electrodes. A finger-shaped source/drain electrode structure was adapted for testing devices. Following is the description of the process. First, an indium tin oxide (ITO) layer of thickness 1500 Å was sputtered and patterned by photolithography as the gate electrode on a glass substrate. Then, a silicon dioxide layer of thickness 3000 Å was prepared by plasma-enhanced chemical vapor deposition at 106.6 Pa and 380 °C. The gases He, O_2 and tetraethylorthosilicate (TEOS) were used with the following respective breakdown of gas quantity: 100, 3500, and 175 sccm. The silicon dioxide layer served as the gate dielectric and the breakdown electrical field was near 4 MV/cm. Then, the source/drain electrodes, also associated with a sputtered ITO layer of thickness 1500 Å, were deposited and patterned. Finally, pentacene, purchased from FULKA Chemical (97^{+}%), was thermally evaporated and transformed into a 1500 Å thickness layer through a shadow mask, to form the active region. The evaporation rate was maintained at 0.5 Å/s and the substrate temperature was fixed at 70 °C at a pressure of 5×10^{-5} Pa.

Throughout the TNLC process, the OTFTs array (backplane) was processed according to the technological process described above. Then, a water-based encapsulation poly (vinyl alcohol) (PVA) layer of thickness 6000 Å was spin coated on it. A spin-coated and rubbed polyimide (PI) layer of thickness 1000 Å was formed to align the TNLC. The two layers also serve as the passivation layer comprising the bottom plate. The top plate was formed by fabricating a sputtered ITO layer of thickness 1500 Å as the common electrodes with the addition of a spin-coated, rubbed polyimide alignment layer of thickness 1000 Å on a glass substrate. Finally, the two plates were assembled by a full sealing of the TNLC at 150 °C.

All the electrical characteristics were measured using a Hewlett-Packard 4155A Semiconductor Parameters Analyzer and a Keithley Model 237 High-Voltage Source-Measure Unit. The basic electrical characteristics and direct current (dc) stress were measured in normal air, in dry air and in a high vacuum.

3. Results and discussion

3.1. Sensitivity to humidity

Fig. 1 plots the influence of the measuring environment on the device performance of pentacene transistors with the bottom-contact configuration. In this bottom-contact device, the pentacene was deposited onto the gate insulator, the prefabricated ITO source/drain electrodes. In ambient air, the device performed poorly with a field-effect mobility (μ) of only 0.018 cm^2/Vs, a threshold voltage (V_t) of -3.3 V, an on/off ratio of order 10^4 and a subthreshold slope (SS) of 5.4 V/decade. The electrical parameters were extracted by applying standard metal-oxide-semiconductor field-effect transistor (MOSFET) equations, which are described in an earlier work [22]. As a next step, the characteristics of the device were measured after it had been stored in dry air for 25 h. The device exhibited better performance with a μ of 0.026 cm^2/Vs, a V_t of -3.3 V, an on/off ratio of 10^6 and an SS of 3.9 V/decade. The performance indicators were

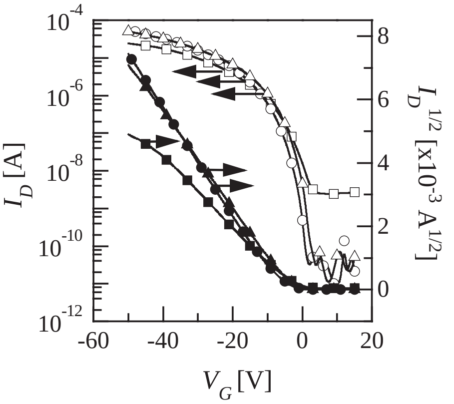

Fig. 1. Log (I_D) – V_G (left axis, open symbols) and $(I_D)^{1/2} - V_G$ (right axis, closed symbols) characteristics of a pentacene transistor measured in air (squares), in vacuum (circles), and in dry air after 25 h of pre-test storage (triangles) with a V_{DS} of -50 V. The channel width and length are 20000 and 57 μm, respectively.