

Short channel effects in polysilicon thin film transistors

G. Fortunato*, A. Valletta, P. Gaucci, L. Mariucci, S.D. Brotherton

IFN-CNR, Via Cineto Romano 42, 00156-Roma, Italy

Available online 2 March 2005

Abstract

Short channel effects have been investigated in n-channel polysilicon thin film transistors. Transconductance degradation has been observed when reducing the channel length L and this effect has been explained with the presence of a parasitic resistance related to residual implant damage. Threshold voltage slightly decreases for channel length around $L=1\ \mu\text{m}$ and simulations confirm that the roll-off of the threshold voltage is expected for $L<1\ \mu\text{m}$. In the output characteristics a stronger kink effect has been observed at short L which, from a comprehensive analysis of the current components, can be attributed to an enhanced parasitic bipolar transistor action.

© 2005 Elsevier B.V. All rights reserved.

Keywords: Polysilicon TFTs; Short channel effects; Kink effect; Parasitic bipolar transistor

1. Introduction

Polycrystalline silicon (polysilicon) thin film transistor (TFT) technology is emerging as a key technology for both active matrix liquid crystal displays (AMLCDs) [1] and active matrix organic light emitting displays (AMOLEDs) [2], allowing the integration of both active matrix and driving circuitry on the same substrate. Integration of other functions should lead to system-on-panel (SOP) technology, requiring, however, a significant improvement in the performance of current polysilicon TFTs. The biggest leverage in circuit performance can be obtained by the reducing channel length, L , from the typical, current values of $L=3\text{--}5\ \mu\text{m}$ to $L=1\ \mu\text{m}$, or less. Therefore, short channel effects in scaled down polysilicon TFTs will have to be controlled in order to allow proper operation of the devices. In this work we have studied the electrical characteristics of devices with channel lengths down to $1\ \mu\text{m}$, by combining experimental data with two-dimensional numerical simulations.

2. Experimental results

The n-channel TFTs used in this work were fabricated at Philips Res. Lab [3] on about 40 nm thick films of excimer laser crystallised polysilicon, using a self-aligned (SA) architecture, in which the source and drain dopant (P) was implanted through the gate oxide, and was activated by a second pass through the excimer laser. The gate oxide was deposited in a PECVD system using SiH_4 and N_2O , and ranged in thickness t_{ox} from $t_{\text{ox}}=45\ \text{nm}$ to $t_{\text{ox}}=150\ \text{nm}$. In Fig. 1a,b typical $I_{\text{d}}\text{--}V_{\text{g}}$ characteristics (Fig. 1a) and normalised transconductance (Fig. 1b), $g_{\text{m}}L$, are shown. It appears evident that for decreasing channel length L the device transconductance is seriously degraded.

In order to investigate the short channel effects in such devices we analysed the threshold voltage, V_{t} , dependence upon L . The threshold voltage V_{t} has been determined as the gate voltage giving a drain current of $I_{\text{d}}=W/L\ 10^{-7}\ \text{A}$, a current level sufficiently low to reduce the effects of parasitic resistance. In Fig. 2 the plot of V_{t} vs. L is shown for three different gate oxide thicknesses and, as can be seen, only a minor V_{t} decrease with decreasing L is observed in the devices with thicker gate oxide. Finally, output characteristics have been measured for different L and compared at relatively low V_{g} (around threshold

* Corresponding author.

E-mail address: fortunato@ifn.cnr.it (G. Fortunato).

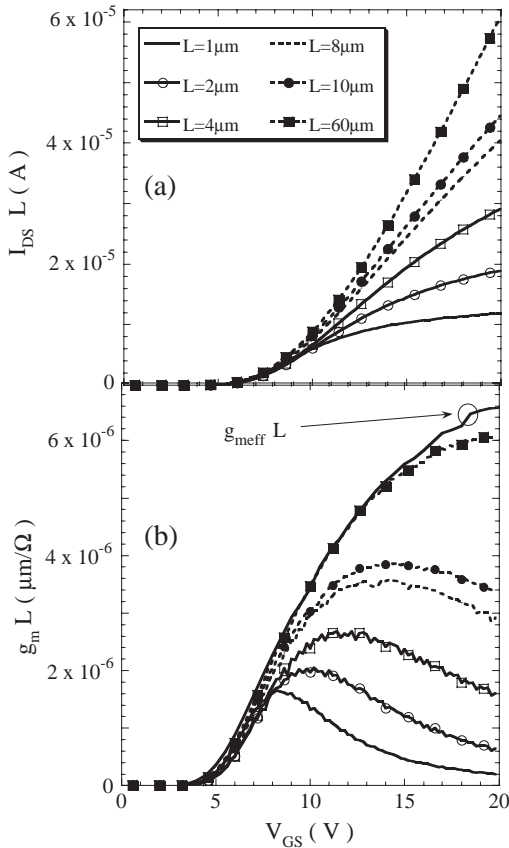


Fig. 1. Normalised transfer characteristics (a) and transconductance (b) vs. gate voltage for SA devices with different channel lengths.

voltage), so that the characteristics were not affected by the parasitic resistance effect. The gate bias, V_g , for the output characteristics measurements was also adjusted to maintain the same low-field normalised output conductance, $g_{d0}L$. As

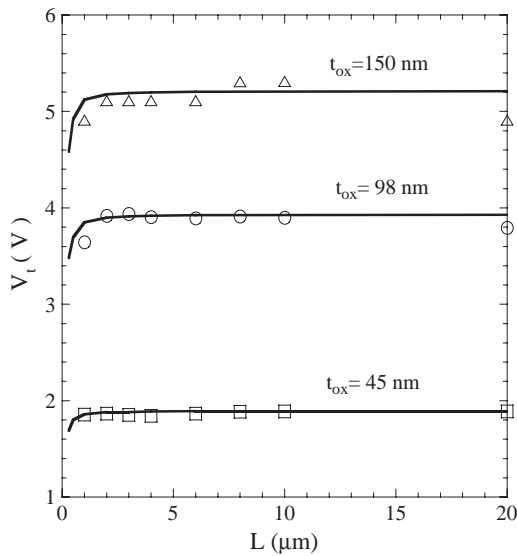


Fig. 2. Experimental (open symbols) and simulated (solid lines) threshold voltages of devices with different channel lengths and oxide thickness (t_{ox}).

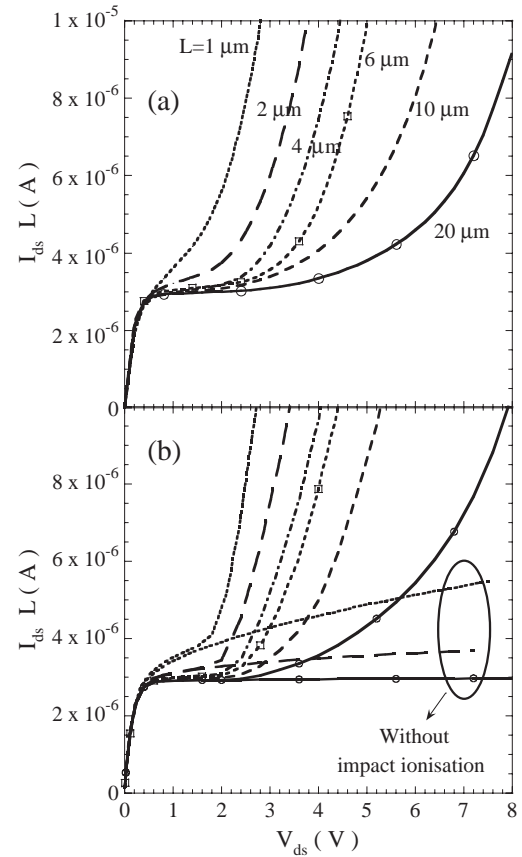


Fig. 3. Experimental (a) and simulated (b) output characteristics for $V_g=2.1$ V (around threshold voltage) and different channel length, L . Simulated characteristics have been calculated by including impact ionisation mechanism and for $L=1, 2$ and $20 \mu\text{m}$ we also reported the characteristics obtained by turning off the impact ionisation.

can be seen in Fig. 3, for TFTs with $t_{ox}=40$ nm, both saturation current and kink effect appear very sensitive to channel length reduction. In particular, for short channel devices, the characteristics no longer saturate and the anomalous current increase occurring at high V_{ds} , called

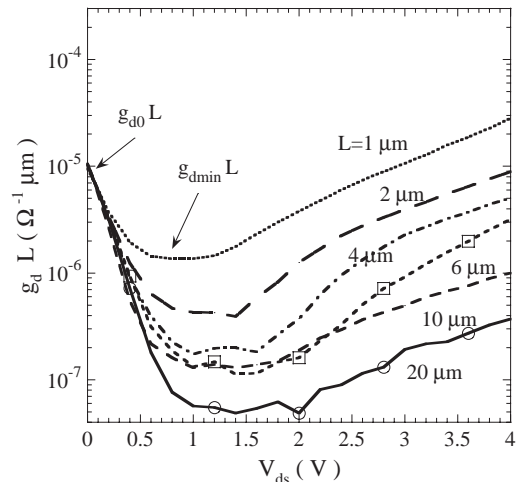


Fig. 4. Normalized output conductance ($g_d \times L$) deduced from data shown in Fig. 3a. Also indicated are g_{d0} and g_{dmin} .

Download English Version:

<https://daneshyari.com/en/article/9812397>

Download Persian Version:

<https://daneshyari.com/article/9812397>

[Daneshyari.com](https://daneshyari.com)