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Improved electrical stability in asymmetric fingered polysilicon thin film transistors

M. Cuscunà*, L. Mariucci, G. Fortunato, A. Bonfiglietti, A. Pecora, A. Valletta

IFN-CNR, Via Cineto Romano 42, Rome 00156, Italy

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Abstract

Recently, we proposed asymmetric fingered polysilicon thin film transistors, where the transistor channel region is split into two zones with different lengths separated by a floating n^+ region, which allows an effective reduction of the kink effect. In this work, we analysed the experimental electrical characteristics by using numerical simulations for a specific channel configuration and then we studied the effects of prolonged bias stress on these devices and conventional non self-aligned thin film transistors. We found that asymmetric fingered transistors are characterized by a substantial reduction of the transconductance degradation induced by hot carrier effect, if compared to conventional thin film transistors. By modeling the device with two transistor in series, we could explain the reduced effects of hot carrier-induced degradation.

Keywords: Polysilicon TFTs; Kink effect; Hot carrier-induced degradation

1. Introduction

The introduction of excimer laser crystallization in polysilicon thin film transistors (TFTs) technology has produced a considerable improvement of device performances. Indeed, achievement of field effect mobility in excess of 100 cm^2/V s [1] has opened the doors to a number of circuit applications of polysilicon TFTs. In particular, full integration of driving circuitry in active matrix liquid crystal displays (AMLCDs) [2] as well as in active matrix organic light-emitting displays (AMOLEDs) [3] is, at present, the application most actively investigated, and, thanks to improved performance, system-on-glass could be eventually fabricated. However, conventional self-aligned polysilicon TFTs present several undesirable effects in electrical characteristics, including large off-current [4], kink effect [5], and hot carrier instabilities [6]. The kink effect increases, in digital circuits, power dissipation and slightly degrades switching characteristics, while in analogue circuit applications, it reduces the maximum attainable gain as well as the common mode rejection ratio. The usual approach to reduce this effect is to limit the impact ionization contribution decreasing the electric field at the drain junction.

Degradation of electrical characteristics related to hot carrier effects (HCE) is, of course, an important issue in polysilicon TFT circuit application. These effects are induced by the presence of intense electric fields at the drain junction, determined mainly by the abruptness of the lateral doping profile. Extensive investigation of HCE in polysilicon TFTs has shown that, similarly to c-Si MOSFETs, device degradation is controlled by the formation of interface states and oxide traps and charge injection in the gate oxide [7,8]. Recently, it has been also proposed that hot carrier-induced defects could be generated at the grain boundaries, creating a damage region at Si/SiO_2 interface, close to the drain junction [8]. In order to minimize the abovementioned effects, asymmetric fingered architecture for polysilicon thin film transistors (AF-TFTs) have been proposed [9], allowing an effective reduction of the kink effect. In this work, we investigated HCE in conventional and AF-TFT-induced prolonged device bias stressing for V_g at the threshold voltage V_t and compared it with the electrical stability of conventional TFT structures.

* Corresponding author. Tel.: +39 6 41522246; fax: +39 6 41522220.
E-mail address: cuscuna@ifn.cnr.it (M. Cuscunà).

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2. Device fabrication

In Fig. 1, both AF-TFT and conventional non self-aligned TFT structures are reported. In the AF-TFTs ,the channel region is split into two zones with different lengths: L_1=8 μm, L_2=2 μm, separated by an n^+ floating region. The devices were fabricated on oxidised silicon wafers. First, a layer of hydrogenated amorphous silicon (a-Si:H), 100 nm thick, was deposited at 350 °C by plasma enhanced chemical vapour deposition (PECVD). Then, a highly doped a-Si:H PECVD layer (25 nm thick) was deposited by PECVD at low temperature (120 °C), using a SiH_4+PH_3 (1%) gas mixture. Source and drain regions were defined by photolithography, removing the n^+ films from the channel regions by using a selective wet etching. Subsequently, the samples were furnace-annealed at 500 °C in N_2 to remove hydrogen. The sample was irradiated by excimer laser and, in this step, the channel region was transformed into polysilicon, and the dopants, present in the source and drain regions, were also activated. After definition of the active layer island, the gate oxide is deposited (150 nm thick) at 350 °C by PECVD from a SiH_4+N_2O+He gas mixture. Finally, contact holes are formed and metal contacts (Al+1% Si), for source, drain, and gate electrodes, are deposited and defined. Gas annealing at 450 °C for 20 min was performed to passivate some of the defects.

3. Electrical characteristics

Electrical measurements were performed on conventional (L=10 μm, W=50 μm) and AF-TFTs devices (L_1=8 μm, L_2=2 μm, and W=50 μm). In Fig. 2, the experimental transfer characteristics, for three different V_{ds} (0.1, 1 and 10 V), for conventional TFT and AF-TFT are compared. As can

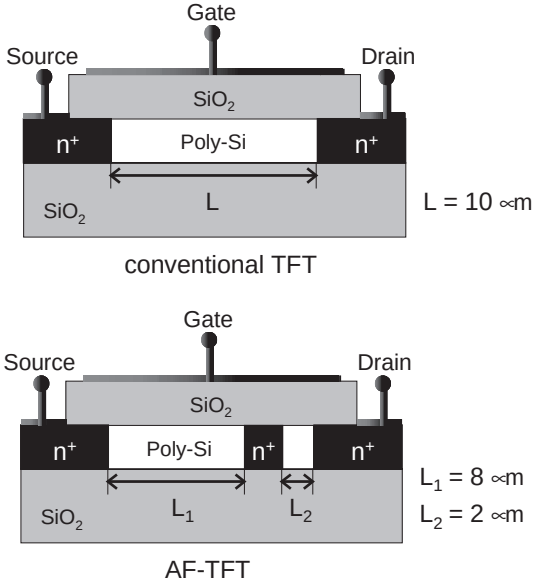

Fig. 1. Schematic of conventional and asymmetric fingered TFT (AF-TFT).

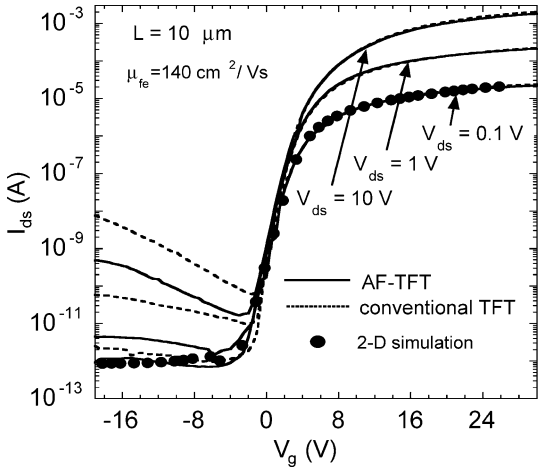

Fig. 2. Experimental transfer characteristics, measured at different V_{ds}, for a conventional TFT (solid lines) and an AF-TFT with L_1=8 μm and L_2=2 μm (dot lines). Simulated transfer characteristic for AF-TFT at low V_{ds} is also shown (closed circles).

be seen, the transfer characteristics are the same for the two TFTs in the on-regime, while in the off-regime at high V_{ds}, there is an appreciable reduction of the leakage current in the AF-TFT, according to what was observed in conventional multiple-gate structures [10]. In Fig. 3a, the experimental output characteristics, measured at different V_g, are shown for the conventional TFT and AF-TFTs. It is evident that a substantial reduction of the avalanche current induced

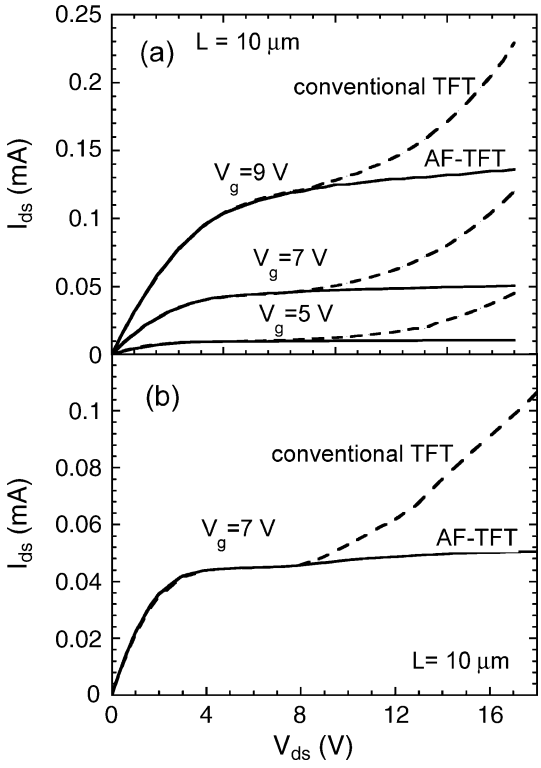

Fig. 3. Experimental output characteristics (a) for conventional TFT (L=10 μm, dashed lines) and AF-TFT with L_1=8 μm and L_2=2 μm (solid line). (b) Simulated output characteristics for conventional TFT (L=10 μm, dashed lines) and AF-TFT with L_1=8 μm and L_2=2 μm (solid line).