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Channel doping effects in poly-Si thin film transistors

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Abstract

The influence of channel doping on the threshold voltage of poly-Si thin film transistors (TFTs) has been investigated using both boron and phosphorus implants. For each dopant type, asymmetric TFT behaviour was seen between enhancement and depletion mode TFTs, with the enhancement mode TFTs always showing a greater shift in threshold voltage for a given dose. From a detailed analysis of the boron-doped samples, using a two-dimensional device simulator, it was demonstrated that the results could be best explained in terms of a non-symmetric density of states, in which the deep trapping state density in the lower half of the band-gap increased with increasing boron concentration. This is the first reported observation in poly-Si of shallow level dopants also introducing deep levels in the majority carrier half band-gap.

Keywords: Poly-Si; TFT; Channel doping; Threshold voltage; Density of states (DOS)

1. Introduction

Poly-Si films usually display an intrinsic n-type nature due to the presence of one or more of the following features: positive charges in the surrounding gate and glass plate capping oxides, a neutral trapping level above mid-gap in the poly-Si, and trace levels of n-type contaminants (presumably Oxygen) in the film itself. As a result of this, it is common practice to lightly dope the channel of poly-Si thin film transistors (TFTs) in order to adjust the threshold voltage, and to obtain complementary metal–oxide–semiconductor (CMOS) transfer characteristics which are symmetrically positioned with respect to zero gate bias. In this paper, we discuss the doping of p- and n-channel TFTs with low doses of both boron and phosphorus, and analyse those results using a two-dimensional (2-D) numerical device analysis program, DESSIS [1]. The experimental results are presented in Section 3, and, for both dopants, the enhancement devices always displayed a greater rate of threshold voltage change with dose than the depletion devices. Such asymmetries, between n- and p-channel transistors, are not expected in MOS field effect transistors (MOSFETs), silicon-on-insulator (SOI), or poly-Si TFTs, and this is confirmed by the two-dimensional (2-D) device simulations presented in Section 4. The only way in which the experimental results for boron-doped devices have been simulated has been by introducing an asymmetric trapping state distribution into the TFT band-gap, with the higher density in the majority carrier (lower) half of the band-gap, which increased with increasing boron concentrations. This resulted in good fits to the measured TFT transfer characteristics, as well as reproducing the threshold voltage dependencies on dose.

Although simulations have not yet been carried out on the phosphorus doped samples, it is anticipated that a similar result will be found to explain the similar experimental data, i.e. increased trapping state density in the majority carrier (upper) half of the band gap.

The hitherto unreported observation emerging from this work is that shallow level dopants introduce further deep trapping levels into the majority carrier half of the band-gap of poly-Si.

2. Sample fabrication

The TFTs were fabricated on Corning 1737 glass substrates, using as a pre-cursor 40 nm thick a-Si:H films

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deposited by plasma enhanced chemical vapour deposition (PECVD), and employed a non-self-aligned (NSA) architecture, in which the source and drain dopants, as well as the channel dopants, were implanted into the material before the laser crystallisation stage. The channel dopants were implanted as P-ions at 10 keV, or BF_2-ions at 13.5 keV, with a dose range from $1–4\times10^{12}$ cm^{-2}. Crystallisation and dopant activation were carried out using a conventional XeCl excimer laser line beam system, with the incident energy density chosen to give optimised, multi-shot super lateral growth conditions [2,3]. This ensured a high level of activation of the dopants, as well as the removal of all initial implantation damage. In addition, the high diffusion coefficients of P and B in molten silicon [4] gave a uniform distribution of the dopant through the film thickness. The PECVD gate oxide was 150 nm thick, and, following final metallisation, the samples were annealed at 350 °C in H_2+N_2 gas mixture to alloy the source and drain contacts, and also to hydrogen-passivate trapping states in the poly-Si film and at the Si/SiO_2 interface. The measurements were taken from TFTs with a channel length of 6 μm and a channel width of 300 μm.

3. Experimental results

The TFT threshold voltage was defined by the intercept, on the V_g axis, of the linear portion of the I_d–V_g characteristic (measured at V_d=0.25 V) extrapolated back to zero drain current, I_d. The variation of threshold voltage with channel doping level, for n- and p-channel TFTs, doped with phosphorus and boron, is shown in Fig. 1a and b, respectively. It will be seen that there was a difference in slope between the n- and p-channel TFTs in each of the two data sets, with the enhancement mode devices showing the greatest slope for both dopants. For the phosphorus doped TFTs, the threshold voltage of the enhancement mode p-channel TFTs changed by -6.6 $V/10^{12}$ phosphorus cm^{-2}, whereas the change in the depletion mode n-channel devices was only -2.2 $V/10^{12}$ phosphorus cm^{-2}. These figures can be compared with the simple, theoretical expectation of -6.9 $V/10^{12}$ cm^{-2} for a delta function charge distribution at the Si/SiO_2 interface. Hence, the p-channel devices are responding largely as expected, whereas the n-channel devices are showing far less than the expected rate of change.

The opposite situation holds for boron doping, in which the rates of change are greater for the n-channel TFTs, at 3.4 $V/10^{12}$ cm^{-2}, compared with 1.3 $V/10^{12}$ cm^{-2} for the p-channel TFTs, respectively. However, these effects are qualitatively the same as seen with phosphorus doping, since the enhancement mode device (the n-channel TFT) is showing the greater slope. The major quantitative difference is the lower absolute value of the slope, suggesting a lower overall level of the boron activation.

Examples of the transfer characteristics of devices doped with 3×10^{12} and 4×10^{12} B/cm^2 are shown in Fig. 2a and b,

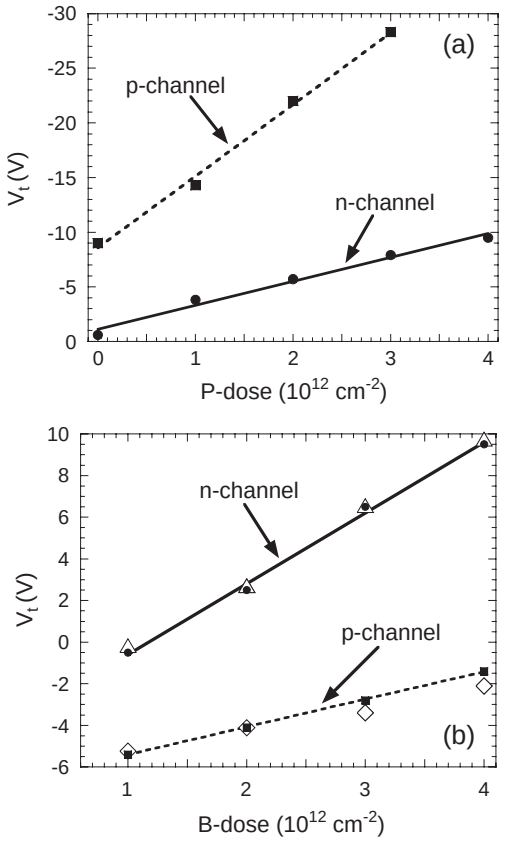

Fig. 1. Variation of poly-Si TFT threshold voltage, measured from linear extrapolation of transfer characteristics, with dose of (a) phosphorus and (b) boron implanted into the channel. Dashed and solid lines are best fit to the experimental V_t-values giving for the p-channel -6.6 $V/10^{12}$ phosphorus cm^{-2} and 1.3 $V/10^{12}$ boron cm^{-2} while for the n-channel TFTs -2.2 $V/10^{12}$ phosphorus cm^{-2} and 3.4 $V/10^{12}$ boron cm^{-2}. Also shown in panel b is the variation of threshold voltage in poly-Si TFTs, calculated using the DOS distribution shown in Fig. 6 (empty rumbles, n-channel, and empty triangles, p-channel).

and the change in threshold voltage with dose is clearly seen. Other features of note in these curves are the increased leakage current and higher cross-over current in the more heavily doped device. These effects, together with the fitted curves, are discussed in Section 4.2.

4. Analysis and simulations

4.1. SOI and MOSFETs

In order to put the above results in context, it is useful to briefly look at the expected trend in behaviour of MOSFET and SOI devices, without the complicating features of trapping states. For MOSFETs (on semi-infinite substrates), the threshold voltage of enhancement mode devices varies with the substrate doping level, N, as $(N)^{1/2}$ [5], whereas similarly doped depletion mode devices will display a high background conductivity, at zero gate bias, due to the substrate doping. As a result of this background conductiv-