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The effect of annealing on $SrTiO_3$ field-effect transistor devices

Keisuke Shibuya[a,*], Tsuyoshi Ohnishi[a,b], Takayuki Uozumi[a], Mikk Lippmaa[a,b], Hideomi Koinuma[b,c]

[a]*Institute for Solid State Physics, University of Tokyo, 5-1-5 Kashiwanoha, Kashiwa, Chiba 277-8581, Japan*
[b]*Combinatorial Materials Exploration and Technology, Tsukuba 305-0044, Japan*
[c]*Materials and Structures Laboratory, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan*

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Abstract

We have investigated the effect of interface states on the performance of a field-effect transistor composed of a $SrTiO_3$ (100) single crystal as a channel and an amorphous $CaHfO_3$ layer as a gate insulator. The amorphous $CaHfO_3$ gate insulator layer, which was grown at a pressure above 1 mTorr by pulsed laser deposition (PLD), had a breakdown field of over 5 MV/cm. The transistors deposited under "hard" ablation conditions, at a laser fluence of ~1.2 J/cm^2, showed a normally on conducting behavior even at zero gate bias. An annealing treatment was found to decrease the interface conductivity by filling oxygen vacancies and the annealed devices exhibited clear enhancement-type transistor action.

Keywords: Field effect; Interfaces; Titanium oxide

1. Introduction

Transition-metal oxide heterostructures have a large potential for new attractive electronic devices; tunneling magnetoresistance (TMR) junctions [1], resistance random access memory (RRAM) [2], or field-effect devices [3]. Furthermore, two-dimensional oxide heterostructures have the potential to surpass the performance of bulk materials, as Ohtomo et al. have demonstrated [4]. However, unclear issues still remain regarding oxide interfaces: for instance, the effects of charge transfer, Schottky contacts, interface states, and atomic diffusion. One approach to develop oxide electronics is to fabricate a simple field-effect transistor (FET) with a performance comparable to a-Si or organic thin film transistors. The FET is one of the most common devices in modern electronics and a good probe for investigating interfaces.

$SrTiO_3$ has attracted a great deal of interest in the world of oxide electronics, not only as a high dielectric constant insulator [5], but also as a wide-gap semiconductor with a band gap of approximately 3.2 eV [6,7]. The Fermi level of $SrTiO_3$ is located close to the conduction band bottom and it is easy to induce conductivity by cation substitution or introduction of oxygen vacancies at a fairly low carrier density of about 10^{18} cm^{-3} [8]. These characteristics become great advantages when $SrTiO_3$ is used as a channel layer of a FET. By combing a wide-gap insulator with non-doped $SrTiO_3$, it is possible to construct metal–insulator–semiconductor (MIS) heterostructures where $SrTiO_3$ serves as a semiconductor [9,10]. The availability of high-quality single crystal $SrTiO_3$ substrates makes it an attractive material for designing such MIS structures. We have previously reported on prominent transistor operation in a single-crystal $SrTiO_3$ field-effect device using an amorphous $CaHfO_3$ gate insulator [10]. In this work, we studied the performance of a $SrTiO_3$ field-effect transistor, which is normally in the conducting state.

Amorphous $CaHfO_3$ was selected for the insulator layer because it is possible to grow atomically flat large-area films. This is significant, because the simple physical masking technique used in fabrication dictated a device with a characteristic size of several hundred μm. Amorphous layers can also be grown at room temperature, thus avoiding $SrTiO_3$ crystal surface modifications that are inevitable during high-temperature growth of epitaxial insulator layers.

* Corresponding author. Tel.: +81 4 7136 3316; fax: +81 4 7136 3319.
E-mail address: kshibuya@issp.u-tokyo.ac.jp (K. Shibuya).

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2. Experimental details

The transistors were fabricated on $5\times10\times0.5$ mm^3 as-supplied $SrTiO_3$ (100) single crystal substrates (Shinkosha) that were NH_4F-HF etched by the vendor and showed atomically flat surfaces and a step-and-terrace structure [11]. As a first step, aluminum source and drain electrodes were thermally evaporated on clean substrates through a stainless steel stencil mask. Aluminum was selected because it has been reported that ohmic contact can be obtained between an aluminum electrode and electron-doped $SrTiO_3$ [12]. Gate insulator layers were grown by PLD at an oxygen pressure of 3 mTorr. A KrF excimer laser (λ=248 nm) operating at 5 Hz was used for ablation. The laser fluence on the surface of the ceramic ablation target was 1.2 J/cm^2, resulting in a deposition rate of 50 pulses per monolayer on the $SrTiO_3$ (100) surface. This laser fluence was higher than what we have reported earlier, because this time our aim was to make the amorphous $CaHfO_3/SrTiO_3$ interface conducting. The target was a polycrystalline ceramic pellet, and the target–substrate distance was 45 mm. The last step of device fabrication was the evaporation of the gate electrodes in exactly the same conditions as the source and drain electrodes. The whole transistor fabrication process was done at room temperature.

The leak current and breakdown field of the amorphous $CaHfO_3$ films were explored in a separate experiment, growing the insulator layers on 0.5 wt.% Nb-doped $SrTiO_3$ substrates. The substrates were pre-annealed at 900 °C for 2 h in air and a step-and-terrace structure was observed. The ablation laser fluence was lowered to 0.5 J/cm^2 for achieving a slow growth rate. Aluminum pads with surface areas of 0.03 mm^2 were evaporated all over the films through a stencil mask after the deposition. All transport measurements were performed using Keithley 487 and 6845 picoammeters and an Agilent precision LCR meter while the devices were mounted in a manual probing station, shielded from light.

3. Results and discussion

3.1. Breakdown field

The breakdown field of amorphous $CaHfO_3$ films was investigated on Nb-doped substrates. The breakdown field was measured at 100 points on the sample surface. A histogram showing the breakdown field distribution is plotted in Fig. 1. White and black bars correspond to films grown at a background pressure of 10^{-5} and 10^{-3} Torr of oxygen, respectively. The film thicknesses were 50 and 45 nm. A higher average breakdown field was achieved in higher-pressure growth, probably due to a smaller amount of oxygen vacancies in the insulator film. The average breakdown field of films grown at 10^{-3} Torr was about 5 MV/cm. On the other hand, at much higher pressures, ~10^{-2} Torr,

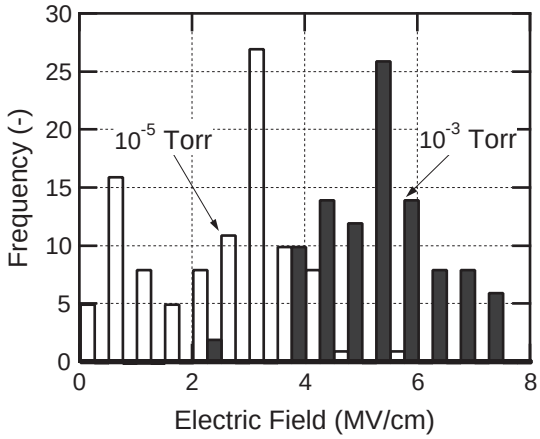

Fig. 1. Histograms of breakdown field distribution of amorphous $CaHfO_3$ films grown on a Nb-doped $SrTiO_3$ (100) substrates. The depositions were done at 10^{-5} Torr of oxygen (white bars) and 10^{-3} Torr (black bars).

surface contamination was observed and the probability of obtaining highly insulating films became smaller. Therefore, deposition at 1–5 mTorr appears to be optimal for amorphous $CaHfO_3$ insulator growth. No significant differences of the dielectric constant were observed with changing deposition pressure.

Typical leak current behavior of a film deposited at 3 mTorr is plotted as a function of applied field in Fig. 2(a). The film thickness was 50 nm. Breakdown was clearly observed at around 4.2 MV/cm. Poole–Frenkel (PF) effect is often used to explain the leak mechanism in insulator layers [13], especially for amorphous materials due to the relatively large number of defect centers present in the energy gap [14,15]. The PF-type conduction was observed in our amorphous $CaHfO_3$ films, as shown in Fig. 2(b). A linear relationship between $\ln(J/E)$ and $\sqrt{E}$ was clearly seen above 2 MV/cm. The leak current in this field range is cause by thermal emission of charge carriers from random Coulombic traps in the film, enhanced by the application of an electric field. From a detailed study of the I–V hysteresis loops, it was found that charging current was predominant when the applied field was below 2 MV/cm.

3.2. FET performance

A schematic drawing of the FET device structure is shown in Fig. 3. The device architecture is similar to conventional FETs, consisting of a channel, a gate insulator, and a gate electrode. Carriers are accumulated at the interface between the $SrTiO_3$ substrate and the amorphous $CaHfO_3$ layer. The physical thickness of the insulator film was 60 nm. The aluminum source and drain electrodes (diagonal hatching in Fig. 3) were about 20 nm thick. The channel length (L) and width (W) of the FET device were 100 and 500 μm, respectively. Electrical contact to the source and drain electrodes was made by wire bonding. The bonding process crushes the 60-nm-thick insulator film and makes contact with the buried aluminium electrodes. The