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Effects of fluorine and chlorine on the gate oxide integrity of W/TiN/SiO_2/Si metal–oxide–semiconductor structure

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Abstract

We investigate the effects of fluorine (F) and chorine (Cl) on the gate oxide integrity of W/TiN/SiO_2 (3 nm)/Si metal–oxide–semiconductor (MOS) structure as a function of W deposition method and post-metal anneal (PMA) process. TiN films were prepared by chemical vapor deposition (CVD) using $TiCl_4$ and NH_3, while tungsten (W) electrodes were prepared by CVD using a WF_6 precursor and by physical vapor deposition (PVD) using a W target. The amount of fluorine ([F]) prepared by CVD-W was two orders of magnitude higher than that prepared by PVD-W. The interface trap density (D_{it}) of MOS capacitor was lower with CVD-W than the one with PVD-W by a factor of two after PMA of 950 °C, resulting in the D_{it} in the mid-10^{10}/eV cm^{-2} range. The higher D_{it}, fixed charges, and oxide trap charges were observed with PVD-W deposition on top of 30 nm-thick CVD-TiN, strongly suggesting damages at the SiO_2/Si interface and SiO_2 even after the rapid thermal anneal at 950 °C and following forming gas anneal. However, a noticeable degradation of gate oxide quality was observed with CVD-W by means of smaller breakdown field, charge to breakdown, and shorter lifetime. The reliability degradation was partially attributed to the Cl from the $TiCl_4$ source, while more severe deterioration was assigned to the F from WF_6 source after the PMA at 650 °C and above.
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1. Introduction

With scaling complementary metal–oxide–semiconductor (CMOS) devices to the sub-90 nm technology node, gate depletion and high gate leakage current have become a significant problem for polycrystalline-Si (poly-Si) gate on ultrathin gate oxide [1–3]. The poly-Si gate depletion in conjunction with boron penetration is especially troublesome for p-type poly-Si on thin SiO_2 (<3 nm). One of the approaches to overcome these problems is to use a metal gate electrode directly deposited on the gate dielectrics [2–14].

A series of advanced researches on direct metal gates were carried out using W [4], Mo [5], WN [6,7], TiN_x [2,9–12], and other metals on SiO_2 [8,13,14]. On one hand, Buchanan et al. [4] reported W midgap metal gate compatible with thin dielectric (~3 nm) and demonstrated symmetric flatband voltages for n- and p-type substrate with a barrier height of 3.70 eV. On the other hand, some interesting results such as generation of interface traps and reliability degradation of MOS devices due to metal penetration and ion damage during the physical vapor deposition (PVD) process were presented [4,5,10–12]. To anneal the aforementioned defects, the MOS structures gated with direct metals were subjected to a post metal anneal (PMA) at high temperatures or in a forming gas anneal (FGA) ambient [4,5,11,12].

Most recently, the feasibility of W/TiN gate stack has been evaluated for conventional 130 nm CMOS technology and beyond [3,9–12]. W/TiN stack is of technological importance because of its midgap work function, low

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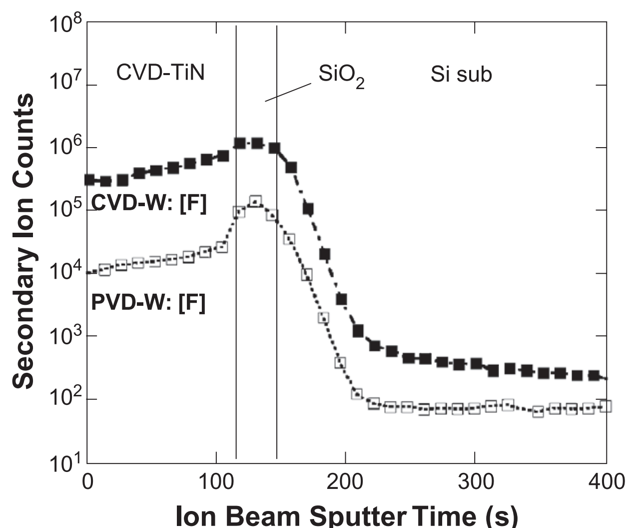

Fig. 1. SIMS profile of F in the $TiN/SiO_2/Si$ stack with two different W depositions. The amount of F is ~3×10^{20} atoms/cm^3 for the CVD-W and <4×10^{18} for the PVD-W.

resistivity and good diffusion barrier properties [7,9]. While PVD-TiN films sputtered at high temperature showed better electrical properties than those prepared at room temperature [3], chemical vapor deposition (CVD)-TiN prepared by $TiCl_4$ and NH_3 demonstrated lower gate leakage and better flat band voltage uniformity than PVD-TiN [10,11]. While the use of CVD-TiN may control the quality of MOS characteristics, the role of upper electrode has not been studied comprehensively. In general, the top electrodes need to have good thermal stability and low resistance. Good step coverage is also required when considering a damascene or replacement gate structure. So far, many of the W/TiN stack evaluations were performed by the PVD-W on various TiN films. However, we selected two different W deposition methods such as CVD-W and PVD-W on the CVD-TiN to evaluate the top electrode effects on the MOS device characteristics for a given PMA. WF_6 is one of the most known precursor materials for CVD-W and has been used in deep contact application because of good step coverage properties, while the fluorine in WF_6 can negatively affect the MOS device performance.

In this paper, we studied the effects of fluorine (F) and chlorine (Cl) on the characteristics of the $W/TiN/SiO_2/Si$ MOS capacitors by comparing two different W metal electrodes prepared by CVD and PVD. This paper focuses on the evolution of defect charges such as interface traps and various defect charges, and evaluates the gate oxide integrity (GOI) during metal gate formation and PMA on controlled SiO_2 (3 nm). We found that CVD method reduced the generation of defect charges over PVD-W, whereas it degraded the GOI characteristics due to the flourine introduced during CVD process and following PMA.

2. Experimental

The substrates were 8-in., (100) oriented p-type silicon wafers with a resistivity of 8–10 Ω cm. After field oxidation for device isolation, a standard pre-gate cleaning step was employed using a diluted-HF final cleaning and deionized water rinse prior to gate oxidation. Controlled gate oxides, SiO_2 (3 nm), were grown in a wet oxidation ambient at 700–800 °C in a resistively heated vertical furnace. As an electrode of metal gate, chemical vapor deposition (CVD)-TiN film (~30 nm) was prepared by thermal reaction of $TiCl_4$ and NH_3 at 550–650 °C. To examine the effect of F on the gate oxide quality of MOS capacitors, W electrodes (~60 nm) were prepared by CVD using a WF_6 precursor at 400 °C with a SiH_4 soaking to enhance the nucleation of W at the initial stage of deposition. In comparison, a sputtering of a W target was also prepared by a DC magnetron sputtering at 200 °C using a plasma power density of 1–2 W/cm^2 as a reference for fluorine-free source. This was followed by photolithography and reactive ion etching to form 4×10^{-4} cm^2 square electrodes. To investigate the effects of PMA on MOS characteristics, the MOS structure was exposed to rapid thermal anneal (RTA) at 650–950 °C in nitrogen for 20 s, followed by a forming gas anneal at 450 °C in 10% H_2/90% N_2 for 30 min.

Electrical characterization of the $W/TiN/SiO_2/Si$ MOS capacitor was carried out in a light free probe station. In

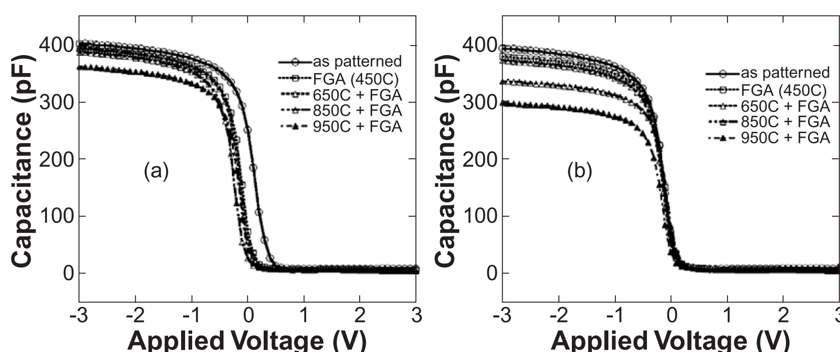

Fig. 2. The high frequency (100 kHz) C–V hysteresis characteristics of the W/CVD-TiN/SiO_2 (~3 nm)/p-Si MOS structures as a function of PMA; (a) PVD-W and (b) CVD-W. The C–V hysteresis traced from inversion to accumulation (+3 V→−3 V) and back to inversion (+3 V).

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