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Application of ultra-high energy boron implantation for superjunction power (CoolMOS^{TM}) devices

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Abstract

Superjunction devices (SJDs) are a novel class of power devices which break the physical limit of silicon with respect to the area-specific turn-on-resistance. SJDs consist of a modified vertical MOSFET structure which is characterized by additional deep pillar-like p-type regions formed inside the $n^{(-)}$ epi-layer below the transistor gate. In the present investigation ultra-high energy boron ion implantation of 2–25 MeV was applied for forming the deep p-type regions laterally structured using Si stencil masks. For energies above 12 MeV the incident ions exceed the Coulomb barrier for Si which leads (i) to a significant gamma and neutron emission during implantation and, (ii) an activation of the wafer and the mask material. However, the most relevant reaction for activation ($^{11}B + {}^{28}Si \rightarrow {}^{39}K(n\alpha) \rightarrow {}^{34m}Cl(\beta, EC) \rightarrow {}^{34}S$) has a half-life time of only 32 min, hence the radiation level of the wafers drops below the critical limit within the processing time. Based on the described technology Infineon Technologies successfully prepared a set of prototype wafers with fully functional high-voltage transistors. Typical blocking capability was approx. 560 V with an area-specific turn-on-state resistance of about 3.85 $\Omega\,mm^2$.

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Keywords: Power devices; Silicon; Ion implantation; Doping; Accelerator; Radiation

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1. The device concept

High-voltage superjunction devices (SJDs), firstly realized by Infineon's CoolMOS™ technology, are a novel class of power devices which break the physical limit of silicon with respect to the area-specific turn-on-resistance value ($R_{on} \times A$) [1]. Such SJDs consist of a modified vertical MOSFET structure characterized by additional deep pillar-like p-type regions formed inside the $n^{(-)}$ epi-layer below the transistor gate, see Fig. 1. Charge compensation between p- and n-type regions leads to an electron accumulation in the drift layer between the p-type columns which results in a reduction of ($R_{on} \times A$) up to a factor of 10 without any loss in the blocking capability. SDJs were introduced into the market between 1998 and 2000 [2–4]. On a commercial scale the vertical stack is presently fabricated with a high effort by repeated cycles of n-type epi-layer growth, masked boron implantation at common energies and subsequent diffusion. There are numerous suggestions for alternative technologies, most of them involving a deep trench structure [5,6]. The novel approach described in this contribution uses ultra-high energy boron implantation to form the p-type pillars. This concept represents a major simplification of SJDs fabrication since the overall number of process steps is drastically reduced.

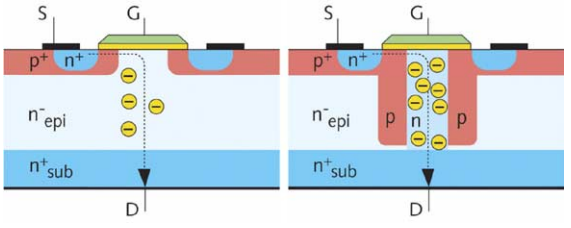

Fig. 1. Schematic cross-sections of a classical MOSFET and a CoolMOS™ power device.

2. Device preparation including masked ultra-high energy ion implantation

The fabrication of CoolMOS™ devices including high-energy boron implantation has been investigated based on the conventional Infineon's MOSFET power device technology. ∅ 6″ Si(0 0 1) wafers with a $n^{(-)}$-type epi-layer ($\rho \sim 2\ \Omega$ cm) of approx. 40 μm thickness have been used. For the patterned implantation of high-energetic boron ions, reusable Si stencil hardmasks were developed by IMS Stuttgart [7]. The hardmasks were fabricated from SOI wafers (500 nm buried oxide, 22 μm SOI). In order to ensure safe masking even

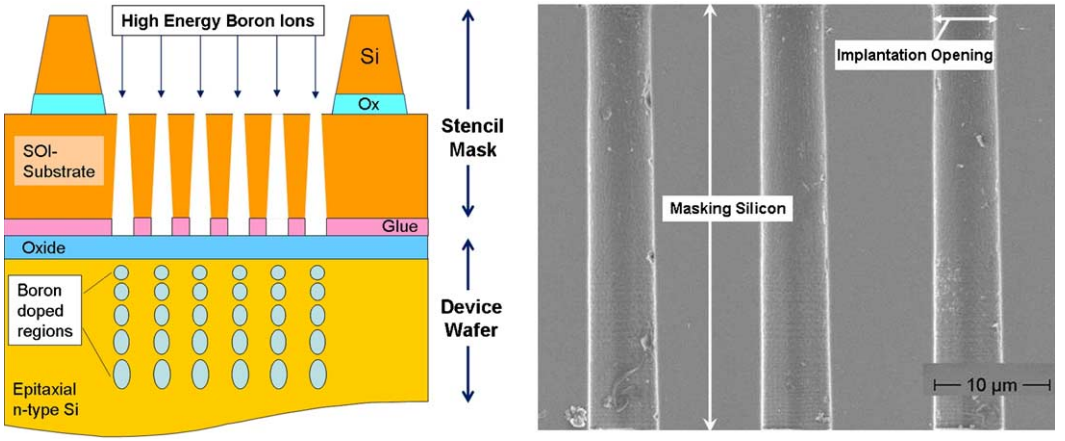

Fig. 2. Sketch of the wafer/mask stack as used for ultra-high energy boron implantation; the right part of the figure shows a cross-sectional SEM-image of the etched Si stencil mask with the implantation openings.