



Poly-Si gate engineering for advanced CMOS transistors by germanium implantation

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Abstract

Standard gate materials are compared to Ge implanted poly-Si and deposited poly-SiGe. It is demonstrated in this paper that the electrical resistance of the gate is significantly reduced via the use of poly-SiGe (from 30% to 40% decrease in resistance). Similarly, we show via specific optimization that localized Ge implantation is also suitable to reduce gate resistance. Physical characterizations are performed to determine the “root” causes at the origin of these improvements. In line with future publications showing strong benefits on CMOS device performance, grain size effects seem to be the main mechanisms explaining the measured improvement.

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1. Introduction

The doping depletion of poly-silicon gate at the dielectric interface is one of the major performance limitations in the standard advanced CMOS transistors. Previous studies [1–3] have shown some performance improvement (electrical oxide thickness reduction and sheet resistance, R_s , decrease) with poly-SiGe gates. In this study, we propose

to evaluate the capability of germanium implantation to modify the electrical behavior of poly-silicon gates. Bang et al. [4] worked on poly-SiGe with 25% and 50% of Ge. They show R_s diminution for boron implanted wafers increased with Ge concentration and R_s augmentation for phosphorus implantation. First, we study the electrical characteristic amelioration by using poly-Si_(1-y)Ge_y ($y < 25\%$) instead of poly-Si. The physical mechanisms responsible for this amelioration are determined. As poly-SiGe gate may induce some integration issues (gate etching, silicide formation, gate oxide integrity...), we have chosen to study

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the capability of replicating such improvement via Ge implantation. Moreover, the implantation offers the possibility to unique advantage of localizing the Ge implantation on specific devices. The appropriated conditions to have low R_s are optimized. To understand the Ge implantation impact, we studied the dopant concentration profiles in the gate materials and their respective grain size.

2. Experimental

$\langle 100 \rangle$ silicon wafers with 20 Å of SiO_2 were used as starting substrates. 1200 Å of polysilicon or poly-SiGe were deposited by CVD (chemical vapor deposition). Different Ge implantations were performed in pure poly-Si with doses ranging from 2×10^{15} at/cm² to 6×10^{15} at/cm². Then, all materials were implanted with P or B with doses ranging between 2×10^{15} at/cm² and 6×10^{15} at/cm². After implantation, the films damages were suppressed and the dopants activated by Rapid Thermal Anneal (RTA) at high temperature (between 1050 °C and 1110 °C). The sheet resistance was measured via a 4-point probe tool all over the 200 mm wafer (48 points). The electrical results are compared with physical observation like concentration profiles and grain size. The dopants profiles were measured via Secondary Ion Mass Spectroscopy (SIMS). These analyses were performed using an ImsWf quadrupole Cameca SIMS instrument with 3 keV Cs^+ primary ion beam for phosphorus and with 2 keV O_2^+ as primary ion beam for boron and germanium. The grain size of the polycrystalline materials was determined via SEM (Secondary Electron Microscopy) after a chemical revelation, $\text{K}_2\text{Cr}_2\text{O}_7:\text{HF}(50\%):\text{H}_2\text{O}$.

3. Results and discussions

3.1. Comparison between poly-Si and poly-SiGe

3.1.1. R_s diminution by using poly-SiGe instead of poly-Si

Using same dopants implantations for poly-Si and poly-SiGe wafers, the R_s values for both materials are shown in Fig. 1 for p-type (a) and n-type

(b) gates. Fig. 1 shows the R_s decrease with the poly-SiGe use. A very significant gain in R_s is measured for both, p-type (40–50%) and n-type (20–40%). High thermal cycle gives smaller R_s values except when implanting phosphorus in poly-SiGe for which the temperature variation (in the range studied here) does not impact the gate resistance.

3.1.2. Dopants concentration profiles

Fig. 2 shows the P profiles in poly-Si and in poly-SiGe for different anneal temperatures.

In poly-Si, the profiles are flat after the anneal illustrating a fast and complete diffusion of P, without any signature of the implantation process. In poly-SiGe, the P diffusion seems to be limited as the presence of Ge may induce strained SiGe films for which the P diffusion is reduced [5]. As seen on Fig. 2(b), for the depth deeper than 60 nm, the P concentration is lower. This depth corresponds to the self-amorphisation depth due to the P implant process. We may suspect that a change in the crystalline structure of the material is at the origin of the change in the P diffusion behavior in the poly-SiGe.

For both, poly-Si and poly-SiGe, there is an accumulation of P at the poly-Si (poly-SiGe) and SiO_2 interface (depth = 120 nm) due to the segregation of P between these two materials. We also observe a significant P out-diffusion as given by the SIMS profiles. The P out-diffusion is most important in poly-SiGe (20%) than in poly-Si (7%).

The concentration plateau of P concentration is lower in poly-SiGe than in poly-Si. The plateau value is lower for high anneal temperature (respectively 2.6×10^{20} at/cm³ versus 3.1×10^{20} at/cm³ at 1110 °C and 2.9×10^{20} at/cm³ versus 3.4×10^{20} at/cm³ at 1080 °C) and due to the dopant out-diffusion which increases with the annealing temperature.

Fig. 3 presents the B ($3 \text{ keV } 4 \times 10^{15}$ at/cm²) profiles in poly-Si and in poly-SiGe for different anneal temperatures.

For both, poly-Si and poly-SiGe, the peak concentration corresponding to the projected range of the implant process (15 nm), is still present after the anneals. For the poly-Si the limit of solubility is reached for anneal temperature

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