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Reliability study of bulk and SOI SRAMs using high energy nuclear probes

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Abstract

The reliability of the bulk and SOI SRAMs was investigated using high energy proton probes with energies of 300–800 keV and operating voltages of 1.5–1.9 V. The soft and hard errors did not occur in the SOI and bulk SRAMs with a proton probe energy of 300 keV. The soft errors in the SOI SRAMs with a body-tie structure occurred with a proton probe energies of more than 350 keV. On the contrary, less soft errors in bulk SRAMs occurred with proton probe energies of 350–800 keV, but many hard errors occurred in the control circuits. The SER in the SOI SRAM depends on the generated excess carriers in the SOI body by proton probe irradiation. The soft errors in SOI SRAMs are suppressed by a higher operating voltage at and near the normal operating voltage.

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Keywords: Silicon-on-insulator; Floating body effect; Reliability; Body-tie; Single event upset; Nuclear microprobe

1. Introduction

Next generation of ultra large scale integrated circuits (ULSIs) need higher speeds and lower power consumption than current ones for system-on-chip (SOC). Silicon-on-insulator (SOI)

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devices are being developed for realization of these demands and for replacing conventional bulk Si devices [1,2]. SOI metal-oxide-semiconductor-field-effect-transistors (MOSFETs) have various advantages over conventional MOSFETs in bulk Si such as soft error free, high speed and low power operation, though there exists the critical issue due to the floating body effect [1]. There are two types of the SOI. One is a partially depleted (PD) SOI and the other is a fully depleted (FD) SOI. The FD-SOI-MOSFET has ideal subthreshold characteristics, no kinks and no floating body effect [3]. However the fabrication of a uniform thin SOI layer is very difficult. By contrast, the fabrication of the PD-SOI-MOSFET is the same as the conventional bulk device processing, though the PD-SOI-MOSFET displays both kinks and the floating body effect. The floating body effect is a problem in the PD-SOI-MOSFET, in which the channel region is insulated from a silicon substrate by buried oxide (BOX) and excess carriers generated from impact ionization by hot electrons and energetic particles are accumulated at the neutral region in the SOI body. These accumulated excess carriers increase the SOI body potential and cause instability in the PD-SOI-MOSFET behavior. This instability is called the floating body effect and is a new issue for soft errors in SOI devices.

One of the simplest ways to suppress the floating body effect in the PD-SOI-MOSFET is to use a body-tie structure, in which body contact electrodes are put on the side of the SOI body and tied to the source contact. The body contact collects holes at the neutral region in the n-type SOI body generated by impact ionization and suppress the floating body effect. However the PD-SOI-MOSFET with a body-tie structure cannot perfectly suppress the floating body effect [4]. In our recent study, the floating body effect in the PD-SOI-MOSFET have been inspected by energetic particle irradiation [5–8]. The effectiveness of body-tie structures was clarified.

In this study, the soft and hard errors in the SOI and bulk SRAMs were investigated by proton probe irradiation with energies between 300 and 800 keV and operating voltages in the range of 1.5–1.9 V.

2. Experimental

Fig. 1 shows the schematic diagram of a PD-SOI-MOSFET with a body-tie structure in a 4 Mbit SRAM. The excess carriers generated in the SOI body were collected by body contact electrodes through a highly doped well under a PTI (partial trench isolation) for suppression of the floating body effect. The process rules of bulk and SOI SRAMs were 0.18 μm. The SOI wafers were fabricated by wafer-bonding. The thickness of the gate oxide was 3.5 nm. The top of the SRAM had four metal and 0.8 μm Si_3N_4 layer. The memory cell included 4n-MOSFETs and 2p-MOSFETs, and the size was 5.4 μm^2.

The amount of the soft error in a 4 Mbit SRAM was monitored after proton probe incidence. The SRAM chips were put in to the vacuum and were shielded with a package resin of the SRAM for uniform probe irradiation and other large peripheral circuits and many cables were in the air. Bulk and SOI SRAMs were irradiated with proton microprobes for 10 s with a beam current of 1 nA, corresponding to 19.2 particles/μm^2 s, using the nuclear microprobe facility of AIST Kansai.

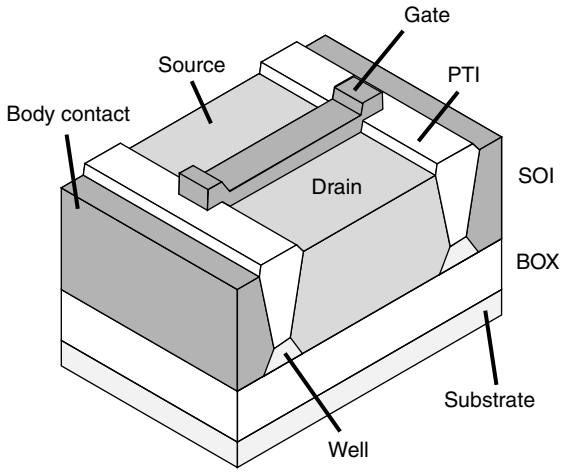

Fig. 1. Schematic diagram of a PD-SOI-MOSFET with a body-tie structure in a 4 Mbit SRAM.