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Design of the front-end analog electronics for the ATLAS tile calorimeter

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Abstract

We describe the design of the analog portion of an electronics system to process signals from the photomultiplier tubes of the ATLAS Tile Calorimeter. The system has a 16-bit dynamic range and is capable of measuring energy depositions in a single calorimeter cell from ~20 MeV to ~1.3 TeV. In order to maintain the calorimeter calibration at the 1% level the system includes a charge injection circuit and a current integrator for use with a cesium source system and with the time-averaged currents produced by the LHC. The system also provides a signal for an analog adder which produces an energy sum for each calorimeter tower. Over 10,000 channels of this system have been constructed and delivered for use.

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1. Introduction

The Tile Calorimeter for the ATLAS experiment at the CERN LHC is used to measure the energy of hadrons produced at polar angles greater than 21°($|\eta|<1.7$). It consists of 9344 cells of iron-scintillator sandwich viewed by two photomultiplier tubes, supplemented by 512 individual scintillators viewed by a single tube. The

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iron-scintillator cells are arranged in towers of approximate size $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$, with three longitudinal subdivisions. Analog signals corresponding to the total energy in each tower are used for the ATLAS Level 1 calorimeter trigger. Details of the calorimeter are described in Ref. [1].

The ATLAS physics performance goals for hadronic jets require an energy resolution $\sigma/E = 50\%/\sqrt{E\,(\mathrm{GeV})} \oplus 3\%$. This performance has been exceeded for single hadrons in test beam studies of a prototype calorimeter [2]. Even more important, the signal-to-energy conversion ratio must be known to 1% or better. To achieve this in the ATLAS environment and over an extended period requires calibration and monitoring of the calorimeter stability at this same level. It will be done by using a pulsed laser system and an electronic charge injection system to make regular measurements of the response of each PMT and of each readout channel over its full dynamic range. The performance of the scintillator and wavelength shifting fibers will be tracked using the signals from single muons passing through the cells, by monitoring the time-averaged signals from individual cells, and by taking special runs with a cesium source used to illuminate successively all 440,000 scintillating tiles in the calorimeter. The readout must measure energy deposition in a single cell ranging from ~20MeV to ~1.3TeV. In the final application several physics channels producing hadronic jets of known characteristics will be used to demonstrate the calorimeter performance.

1.1. Electronics requirements

These requirements place stringent demands on the design of the front-end electronics. The analog portion of the electronics must be mounted as close as possible to the photomultiplier tube (PMT) and fulfill the following functions:

(1) shape the fast PMT signal to the requirements of the 10-bit, 40 megasample per second (MSPS) ADCs used to digitize the signal at the LHC bunch crossing rate,
(2) produce two linear outputs with relative gain of 64 and hence an overall 16-bit dynamic range using two 10-bit ADCs,
(3) inject test signals with similar properties to the PMT signals and of precisely known amplitude over the full dynamic range of the readout,
(4) integrate the PMT signal for use with the cesium source system and for monitoring the PMT current produced by minimum bias beam–beam interactions,
(5) produce a signal for the analog adder used to determine the total energy in a calorimeter tower,
(6) be controlled and configured by a low speed digital bus.

A single printed circuit board called the "3-in-1" card has been designed with these characteristics. Its block diagram is shown in Fig. 1. The individual sections will be discussed below.

The digital portion of the readout for each channel is located approximately 20 cm from the analog portion and consists of a pair of commercial 40 MSPS ADCs together with a custom digital memory chip to buffer the ADC outputs until the Level 1 trigger signal is available. The digital system has been described elsewhere [3].

1.2. Mechanical configuration

The front-end electronics for the Tile Calorimeter is located in 3-m-long electronics drawers at the outer radius of the cylindrical calorimeter. There are two such drawers for each 6-m-long barrel module and one for each extended barrel module. The drawers contain the PMTs, high-voltage distribution system, and the front-end analog and digital electronics. For events satisfying the Level 1 trigger the digitized data is transfered by optical link to off-detector readout driver modules (RODs).

The front-end analog electronics described in this paper is mounted on the voltage divider of each PMT in a drawer. It is built on a 7 cm × 4.7 cm printed circuit board located inside the steel shield of the PMT. Power and control signals are supplied over a flat cable connected to a 2.7-m-long Mother Board system. Differential fast analog signals are output to the digitizers over 22-cm-long shielded pairs.