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The experimental analysis and the mechanical model for the debonding failure of TSV-Cu/Si interface

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ABSTRACT

We have investigated the debonding failure of the through-silicon via (TSV)–Cu/Si interface during annealing treatment at 425 °C. The interface microstructure was characterized by two parameters: the TSV–Cu/Si interface roughness and the Cu seed layer grain size. Scanning electron microscopy observation of the cross-section of the TSV–Cu/Si interface was performed to analyze the effect of the interface microstructure on its microcrack failure. In addition, qualitative numerical simulations were performed to investigate the effect of the TSV–Cu/Si interface roughness and Cu seed layer grain size on the overall response of the TSV–Cu/Si interface crack. The experimental results indicate that most of the TSV interfacial cracks propagate along the Cu seed layer after annealing, and the crack length of the TSV–Cu/Si interface increases with increasing interface roughness and Cu seed layer grain size. The numerical simulation is constructed to reveal the interfacial crack mechanism, and the results suggest that the stress concentration in the Cu seed layer which influence by interface roughness and Cu grains size is the main driving force for interfacial cracking. Based on the experimental and simulation results, guidelines for controlling the TSV-Cu/Si interfacial cracking from the perspective of the TSV manufacturing process are proposed.

1. Introduction

Through-silicon via (TSV) is a promising candidate to perform three-dimensional (3D) integration, which is mainly used in vertical interconnection of stacked chips for homogeneous or heterogeneous system integration [1]. For a shorter interconnection length between multiple stacked conventional components, TSV technology can produce products with higher electrical performance, higher density, and lower weight. However, there are many thermal reliability issues for TSV technologies, such as the scallop-free silicon etching process [2], Cu overburden and void-free filled Cu TSV [3], Cu protrusion [4–6], TSV wafer warpage [7,8], TSV wafer thinning [9], TSV backside via revealing [10], and the bonding/debonding process [11].

Because the TSV–Cu/Si interface reliability may directly lead to electric leakage [12,13] and breakdown [14–16] of the whole 3D integrated circuit (IC) package, TSV–Cu/Si interface integration plays the most important role in the TSV reliability in the 3D IC package. Cu expands much faster than the surrounding Si substrate when heated owing to the mismatch of the coefficients of thermal expansion (16.7 ppm/°C for Cu and 2.3 ppm/°C for Si) during the manufacturing process. This creates severe tensile and shear thermomechanical stresses at the TSV–Cu/Si interface, which is the main driving force for interface cracking [17,18].

Dutta [14,19] pointed out that there are two types of deformation mechanisms depending on the ramp rate of the temperature: frictional sliding and interfacial sliding. Many researchers have attempted to reveal the mechanism of TSV–Cu/Si interfacial failure by introducing the crack energy release rate method into numerical simulations [20–22]. However, owing to the lack of information about the location of the weak interface, the crack propagation path can only be simulated by considering the location of the pre-embedded defects, which makes it difficult for the model to characterize the effect of the inherent microstructure of the interface on interface cracking.

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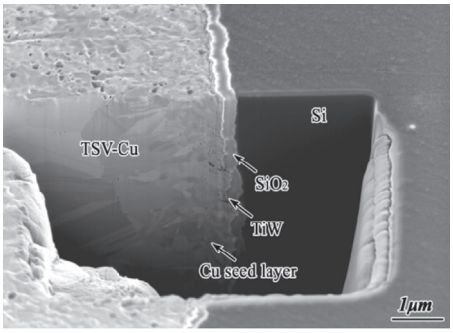
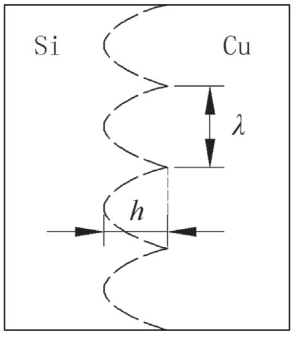
Table 1
Test samples prepared by different electroplating parameters.

Level set	Current density	Additive concentration[a]
HH	1.5ASD[b]	15 mL/L
HL	1.5ASD	10 mL/L
LH	1.0ASD	15 mL/L
LL	1.0ASD	10 mL/L

[a] The additive is kind of polymer material.
[b] Average current density (ASD) = amperage power (Amp)/plating area (dm^2).



a) SEM image of TSV-Cu/Si interface profile



b) Characteristics of TSV-Cu/Si interface

Fig. 1. SEM images of the TSV-Cu/Si interface.

In this study, we investigated debonding failure of the TSV–Cu/Si interface during annealing treatment at 425 °C through experiments and simulations. The debonding behavior of different microstructured TSV–Cu/Si interfaces was experimentally investigated. Finite element simulations were performed to reveal the mechanism of interface fracture. Based on finite element analysis, the effects of the interface roughness and Cu seed layer grain size on the TSV–Cu/Si interface crack behavior are discussed.

2. Experimental procedures

The test samples were fabricated on a 100 mm wafer. The TSV diameter, depth, and pitch were 30, 100, and 200 μm, respectively. An insulating layer (SiO_2), a barrier layer (TiW), and a Cu seed layer were sequentially deposited on the via sidewall. To investigate the effect of the current density and additive concentration on the crack behavior of the TSV–Cu/Si interface, two levels of current densities and two levels of additive concentrations were selected to electroplate Cu into the silicon via. In total, four sets of samples were fabricated, as listed in Table 1. The four sets of samples are called HH (high current density and high additive concentration), HL (high current density and low additive concentration), LH (low current density and high additive concentration), and LL (low current density and low additive concentration). After the plating filled, the standard chemical mechanical polishing process was performed to remove the residual overburden Cu on the wafer surface so that the Cu could freely deform during the following annealing process.

A vacuum annealing furnace with argon gas ambient was used in the annealing process. The temperature was ramped from 25 to 425 °C, and then held at 425 °C for 30 min. To investigate the effect of the ramp rate on the crack behavior of the TSV–Cu/Si interface, three ramp rates were used in the annealing process: 10, 1.2, and 0.6 °C/min.

To investigate the debonding behavior of the TSV–Cu/Si interface during the annealing process, scanning electron microscopy (SEM) observation of the interfaces was performed before and after the annealing process with an FEI Helios NanoLab 600 FIB–SEM dual-beam system with a Ga ion source, which provides both material removal for TSV–Cu/Si interface cross-section preparation and SEM for nondestructive imaging and analysis. A 4 μm deep interface cross-section in the as-electroplated TSV was obtained, as shown in Fig. 1(a). It is clear that the TSV–Cu/Si interface consists of multiple layers, including a SiO_2 insulation layer (0.5 μm), a TiW barrier layer (0.1 μm), and a Cu seed layer (2 μm). The scallop topography of the interface sidewall introduced by the Bosch process is also observed in Fig. 1(a). To quantitatively characterize the roughness of the TSV–Cu/Si interface, the wavelength λ and peak amplitude of the scalloped interface h are defined in Fig. 1(b). The interface roughness can be expressed as h/λ.

3. Observation of TSV–Cu/Si interface deformation

The TSV–Cu/Si interface debonding behavior was investigated at three test points for each sample annealed at a different annealing temperature ramp rate, as shown in Figs. 2–5 for the HH, HL, LH and LL samples, respectively.

For the HH sample (Fig. 2), three test points show no cracking at the interfaces, including two test points annealed with a ramp rate of 10 °C/min and one test point annealed with a ramp rate of 0.6 °C/min. Three test points show partial cracking at the interfaces, including one test point annealed with a ramp rate of 10 °C/min and two test points annealed with a ramp rate of 0.6 °C/min. Three test points show complete cracking at the interfaces, which were all annealed with a ramp rate of 1.2 °C/min. For the HL sample (Fig. 3), no well-bonded TSV–Cu/Si interface is observed. Three test points show partial cracking at the TSV–Cu/Si interface, including one test point annealed with a ramp rate of 10 °C/min, one test point annealed with a ramp rate of 1.2 °C/min, and one test point annealed with a ramp rate of 0.6 °C/min. The other six test points show complete cracking at the interfaces in the SEM observations. For the LH (Fig. 4) and LL (Fig. 5) samples, the interfaces of all nine test points are completely cracked in the SEM observations. Energy dispersive spectroscopy analysis indicates that all of the cracks propagate within the Cu seed layer. A similar failure mode has been reported in many other studies [23–26].