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Mission profile-based assessment of semiconductor technologies for automotive applications

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ABSTRACT

Semiconductor technology has to be qualified under the harsh temperature conditions required by the AEC-Q100 qualification standard before it is applied in the automotive sector. In this paper, we propose a framework to assess different semiconductor technologies for typical automotive electronics components considering both AEC-Q100 temperature specifications and real world automotive environmental temperature profiles as given by mission profiles. The results of the use-case on SRAM indicate that the conventional qualification process based on AEC-Q100 significantly underestimates the reliability of advanced semiconductor technologies and prevents their application in automotive electronics. Qualification based on AEC-Q100 also slightly underestimates the power and performance, however, the amount of underestimation reduces by technology scaling. In addition, our analysis shows that technology scaling does not lead to a performance boost in typical automotive applications due to severe reliability challenges of advanced technology nodes in automotive environments. As a consequence, we consider mission profile-based technology assessment as a promising alternative to the qualification of semiconductor technologies in automotive applications.

1. Introduction

Introducing new functionalities such as driver assistance or automated driving has increased the performance demand of cars in recent years [1]. The performance of the cache subsystem is one of the main factors to determine the performance of embedded systems used in automotive electronics [2]. Static random access memory (SRAM) is used in caches due to its high performance and reliability. To fulfill the increasing demand for performance in automotive applications, it is necessary to use advanced deep sub-micron semiconductor technologies in SRAM cells. However, this leads to severe reliability challenges. The reliability of advanced technology nodes is limited mainly by increasing impacts of process variation and aging phenomena such as hot carrier injection (HCI) and positive/negative bias temperature (PBTI/NBTI) [3,4].

Process variations occur during the manufacturing step for semiconductors and result in inter-/intra-die device parameter variations [5]. On the other hand, aging gradually degrades the device characteristics w.r.t. the environmental conditions and functional loads leading to circuit malfunction [6]. High reliability and lifetime requirements of automotive products and harsh environmental conditions in the presence of process variation and aging set significant limits to the applicability of advanced technology nodes in cars.

To determine the suitability of a new technology for automotive applications, it needs to be qualified w.r.t. requirements imposed from the automotive industry. The AEC-Q100 qualification standard defines a set of failure mechanism-based stress tests, reference test conditions and qualification requirements for integrated circuits (ICs) in the automotive industry [7]. Aging tests for NBTI are conducted under worst case temperature extremes specified as AEC-Q100 temperature grades. This overburdens the qualification of advanced CMOS technologies for automotive electronics and increases their time to market.

In recent years, mission profiles have been used in the automotive industry to capture functional and environmental workloads such as ambient temperatures [8-10]. Unlike AEC-Q100 temperature grades, mission profiles are extracted for a particular mounting location and driving profile. They contain realistic environmental conditions rather than just extreme temperatures which do not occur in the field. Using mission profiles instead of extreme temperatures allows the application-specific qualification and adaptation of new technologies in automotive

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electronics. Adapting new technologies boosts performance and enables the realization of advanced functionalities in the next generation of self-driving cars.

In this work, we propose an approach to assess semiconductor technologies for specific application requirements. As a typical industrial example we apply the approach to assess SRAM cells for automotive applications taking into consideration the impact of both process variation and aging. Unlike AEC-Q100, which uses the maximum temperature for reliability tests, here we use the temperature distribution collected by an automotive OEM for different customer characteristics. The results of our reliability assessment show that the requirements from the AEC-Q100 qualification standard are significantly overestimated. On the other hand, using AEC-Q100 qualification standard leads to underestimation of power and performance. Hence, we propose the use of mission profiles for assessing new semiconductor technologies in automotive applications. The contributions of this paper can be summarized as:

- A framework for the application-specific assessment of semiconductor technologies based on mission profiles and AEC-Q100 temperature grades
- Proposal of a suitable temperature model in mission profiles
- Evaluation of the impact of technology scaling in automotive electronics
- Analysis of the limitations of AEC-Q100 in technology assessment compared to mission profiles

The paper is organized as follows: Section 2 provides background information about AEC-Q100, process variation, aging, and mission profiles. Section 3 introduces our proposed framework for the application-specific assessment of semiconductor technologies based on mission profiles and AEC-Q100 temperature grades. Section 4 discusses the transistor-level analysis followed by Section 5 which presents the reliability, power, and performance assessments of SRAM. Finally, Section 6 summarizes and concludes the paper.

2. Preliminaries

2.1. AEC-Q100 qualification

The Automotive Electronics Council (AEC) introduced the AEC-Q100 standard for qualification of automotive semiconductor components. To be qualified in compliance with AEC-Q100, a new semiconductor technology has to pass a set of wear-out failure mechanisms such as NBTI. Tests in AEC-Q100 are categorized as six Test Groups and each considers different aspects of reliability from die to package level. Test Group D considers die fabrication reliability and considers aging factors such as HCI and NBTI.

The qualification is carried out for one of the five temperature grades defined in the AEC-Q100 standard under worst-case conditions. This means that for a phenomenon such as NBTI which accelerates at higher temperatures the device should be qualified at maximum temperature in the respective temperature grade. Table 1 represents minimum and maximum temperature for each temperature grade.

Table 1
AEC-Q100 temperature grades.

Grade	Min. temperature	Max. temperature
0	−40°C	150°C
1	−40°C	125°C
2	−40°C	105°C
3	−40°C	85°C
4	0°C	70°C

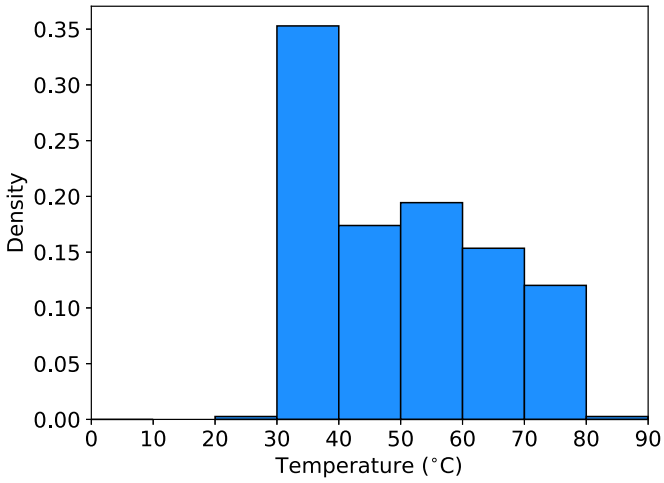

Fig. 1. Ambient temperature distribution of an ECU in the city commuter mission profile.

2.2. Mission profile

A mission profile (MP) contains application-specific functional loads and environmental conditions for a specific component [8]. For example, a mission profile can contain the ambient temperature data of a certain electrical control unit (ECU) that has been collected by a car manufacturer for a specific customer group such as city commuters, under certain operation conditions occurring at their mounting point. Fig. 1 shows the ambient temperature distribution represented by a histogram for an ECU through the lifetime of the device. This data is extracted from a city commuter mission-profile.

Unlike temperature grades that contain only minimum and maximum values, temperature data in mission profiles provide realistic and more detailed characteristics. Therefore, using mission profile data for reliability assessment can give a more realistic insight on the reliability of devices and reduce the unnecessary guard bands.

2.3. Process variation

Variation of key parameters of a CMOS transistor such as the dopant concentration, channel length and width during fabrication affects its performance. Random Dopant Fluctuation (RDF) is considered to be the major source of process variation in CMOS technology nodes below the 90 nm node [11]. The variation induced by RDF can be modeled by the variation of threshold voltage [12]. This threshold voltage variation is inversely proportional to the square root of the transistor area as shown in Eq. (1).

$$\sigma V_{th} = \frac{k}{\sqrt{W \times L}} \tag{1}$$

In Eq. (1), k, W, and L are the technology constant (similar to $A_{V\ T}$ in Pelgrom's area-related mismatch model [13]), the width and length of the transistor respectively. Since the transistor size shrinks in each new technology node, the impact of process variation increases as the technology scales.

2.4. NBTI

NBTI has become a major reliability issue in advanced CMOS technologies. It results in threshold voltage variation and impacts the performance of PMOS transistors. In NBTI, there are two phases called stress and recovery. During the stress phase the transistor is on and the device degrades. During the recovery phase the transistor is off and the degradations of the device recover to some extent. In this paper we use the Reaction-Diffusion (RD) model presented in [14] for modeling the