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Methodology of determining the applicability range of the DPL model to heat transfer in modern integrated circuits comprised of FinFETs

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ABSTRACT

The main aim of this paper is to present the methodology for calculating the applicability range of the Dual-Phase-Lag model in integrated circuits (IC) made of different materials. Furthermore, analyses of requirements for using the Dual-Phase-Lag instead of the Fourier-Kirchhoff heat transfer model are described. All considerations are based on a transistor elementary cell including FinFETs in modern ICs. The obtained results have been analyzed in detail and compared. Moreover, the paper shows an important correction to the Neumann boundary condition required for consistency with the Dual-Phase-Lag equation. In addition, the simplified Dual-Phase-Lag model has also been presented in this paper. It is based on both the classical Fourier-Kirchhoff methodology and Dual-Phase-Lag approach. However, significant improvements related to time lags approximation have been proposed. This simplified model can be implemented in Finite Difference Method and Finite Element Method simulators based on two conjugate diffusion equations. Finally, the temperature distribution inside one- and three-dimensional FinFET structures has been determined based on Fourier-Kirchhoff and Dual-Phase-Lag models.

1. Introduction

Recently, analyses and thermal modelling of modern integrated circuits have been a very popular research area. Proper operation of these electronic structures depends on many different factors. Thus, the ability to estimate with high accuracy temperature distribution in the newest electronic devices is very significant for the reliability of many appliances. Especially nowadays, due to the continuous miniaturization of electronic structures, many malfunctions and much damages occur because of thermal issues [1,2]. Designers and producers have to take into account thermal phenomena which appear in nanometric structures. For this reason, thermal simulations are crucial in this context. Moreover, proper prediction of the temperature distribution in new electronic structures is highly necessary. To obtain a high level of accuracy, different approaches for thermal modelling and other thermal models, which take into consideration physical phenomena characteristic of very small structures, are being developed. The classical thermal model, which is based on the Fourier-Kirchhoff equation, is used frequently for fast power devices and nonlinear heat-transfer, e.g. [3,4] where the characteristic length is 10 times bigger than the heat carrier mean free path (with a Knudsen number of $K_n < 0.1$, see [5,6]) and the physical time scale of the considered heat transfer process is bigger than the heat relaxation times (see τ_T, τ_q in Table 1 and [5,7,39]). Unfortunately, the Fourier-Kirchhoff model is inaccurate for both nanosized electronic structures as well as for very fast power devices [13–15]. Thus, in this paper, a thermal model called Dual-Phase-Lag (DPL) is considered. This model, established by Tzou [6], appeared in the 1990s. The diffusion heat transfer, thermal wave, as well as phonon-electron averaged interaction behavior can be described using time lag terms τ_q and τ_T in the DPL model (see Eq. (1)). However, employing that approach can cause a few problems. One of them is the fact that great computational complexity is observed, which has a significant influence on the time needed for simulation. This can be longer than in the case of the Fourier-Kirchhoff model. Moreover, how applicable that new methodology well as the range of its usage, not well known currently. Thus, the main aim of this paper is to present and analyze the applicability range of the Dual-Phase-Lag model in thermal simulations (Table 7 with Figs. 1 and 2). This approach has been presented with a proposed second-type boundary condition, see Eqs. (2a) and (4). Neither the applicability range of the DPL model nor the new proposed second-type boundary condition has been investigated in [6]. Moreover, another very important aspect focuses on the proposition of a modified model, which relates to Fourier-Kirchhoff and Dual-Phase-Lag model assumptions (see Table 7 with Figs. 3 and 4). This new modified model also suggests a significant improvement of the DPL equation presented in [6]. All thermal analyses and simulations have referenced

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Table 1
Investigated structure material properties at 300 K based on [6,8–12].

Material properties	Material				
	Silicon Si	Platinum Pt	Silicon dioxide SiO_2	Copper Cu	Lead Pb
Density ρ [kg/m^3]	2330.00	21,450.00	2220.00	8900	11,340.00
Specific heat c_p [J/(kg·K)]	712.00	133.00	745.00	382	129.00
Ther. conductivity k [W/(m·K)]	148.00	71.60	1.38	386	35.30
Ther. diffusivity $\alpha{\cdot}10^6$ [m^2/s]	89.20	25.10	0.83	1.01	24.10
τ_q [ps]	3[a]	0.0916[b]	3[c]	0.4348 [6]	0.1670 [6]
τ_T [ps]	60[a]	2.6[b] [7]	60[c]	70.833 [6]	12.097 [6]

[a] The preliminary values of semiconductor time lag terms have been proposed based on [6]. The values for a bulk silicon as well as the silicon quantum can be calculated from the equation $\tau_T = 9\tau_N/5$ and $\tau_q = \tau_U$, where τ_N and τ_U are the averaged relaxation normal and umklapp times in phonon scattering process (see [11]). The empirical approach to measurement is presented in [21,36].

[b] The preliminary values of metal time lag terms have been estimated from equation $\tau_T = c_l/G$ and $\tau_q = G^{-1}/(c_l^{-1} + c_e^{-1})$, where G is the phonon-electron coupling factor, c_l and c_e are the specified heat of phonons and electrons respectively, see [5,9,10]. It was also assumed that theoretical value of the specified heat of phonons is as follows: $c_l = 2.906152\cdot(\pi/(6\cdot(3.1912\cdot10^{-10})^3))\cdot1.38064852\cdot10^{-23}\,\mathrm{Jm^{-3}K^{-1}} = 350{,}916\,\mathrm{Jm^{-3}K^{-1}}$ based on [5,7].

[c] The preliminary values of insulator time lag terms have been proposed based on [6]. The values $\tau_T = 2$ ps and $\tau_q = 10$ ps for heat transport process in the 3-D fractal geometry have been proposed in [7] based on [33], but lagging response time for amorphous media is mainly dependent on material density as well as fractal dimensions, therefore the empirical approach to measurement should be considered [21,36].

transient electric simulations of inverter gates based on predictive methodology for a low-standby power FinFET transistor manufactured in a 14 nm technology node [16]. The presented investigations are significant for their proper employment of the Dual-Phase-Lag model for modern ICs and also for reducing the simulation time.

2. Approach in the thermal domain for 1-D space

This section concerns a description of the investigated Dual-Phase-Lag model and analyses in the frequency domain. Equations, which describe the problem, can be expressed as follows:

$$\begin{cases} c_v\frac{\partial T(x,t)}{\partial t} = -\nabla\cdot q(x,t) + g(x,t) \\ q(x,t) + \tau_q\frac{\partial q(x,t)}{\partial t} = -k\left(\nabla T(x,t) + \tau_T\frac{\partial}{\partial t}\nabla T(x,t)\right) \end{cases} \quad (1)$$

where c_v expresses volume-specific heat capacity, $T(x, t)$ means temperature rise distribution over ambient temperature, $q(x, t)$ describes heat flux density vector, $g(x, t)$ is power generation per unit volume, k represents thermal conductivity and τ_T and τ_q are temperature time lag and heat flux time lag, respectively. It should also be mentioned that this model and time-lag parameter formulas can been derived from the Boltzmann Transport Equation [17,18] (for semiconductors, for more information on other materials see Table 1). During the investigation, the following assumptions regarding boundary and initial conditions were made for 1-D space:

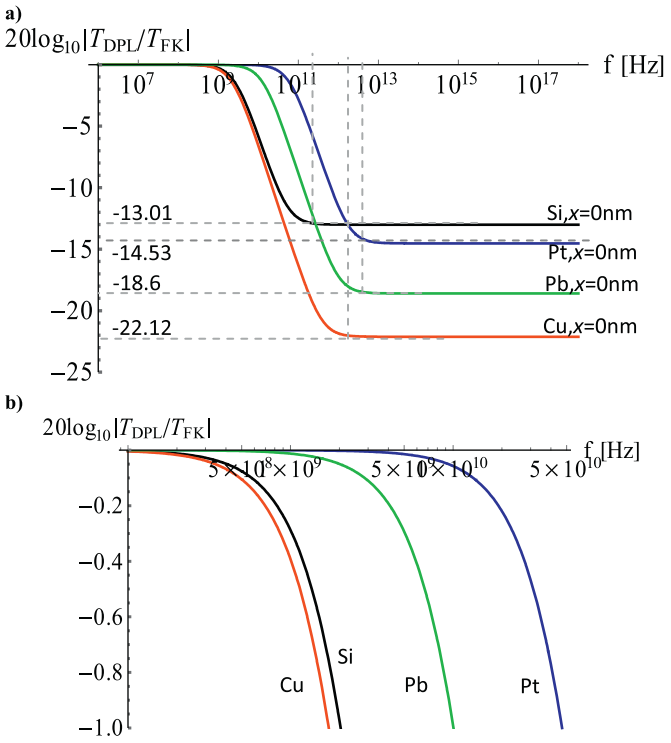

Fig. 1. Comparison of amplitudes of the solution for the 1D Cartesian DPL $|T_{DPL}(f)|$ and FK $|T_{FK}(f)|$ model at $x = 0$ nm for different investigated materials (Si, Pt, Pb and Cu).

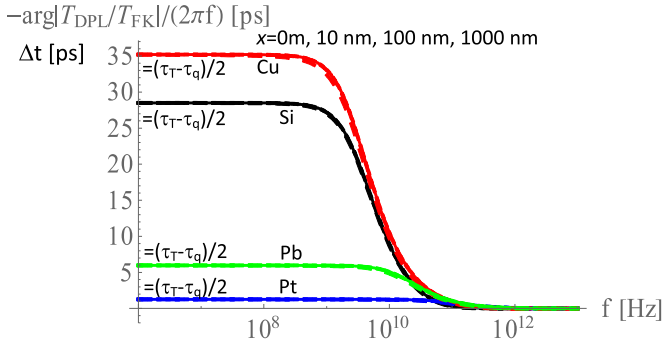

Fig. 2. The time-delay of the 1D Cartesian DPL equation in relation to the 1D Cartesian FK equation for different distances x and different investigated materials (Si, Pt, Pb and Cu).

$$q(x,t)|_{x=0} + \tau_q\frac{\partial q(x,t)}{\partial t}\bigg|_{x=0} = = -k\nabla T(x,t)|_{x=0} - k\tau_T\frac{\partial\nabla T(x,t)}{\partial t}\bigg|_{x=0} \quad (2a)$$

$$q(x,t)|_{x=0} = \delta(t) \quad (2b)$$

$$T(x,t)|_{x\to\infty} = 0 \quad (2c)$$

$$q(x,t)|_{x\to\infty} = 0 \quad (2d)$$

$$T(x,t)|_{t\le0} = 0 \quad (2e)$$

$$q(x,t)|_{t\le0} = 0 \quad (2f)$$

$$g(x,t) = 0 \quad (2g)$$

where $\delta(t)$ means the Dirac delta function. It should also be mentioned that Eq. (2a) contains an important correction to the Neumann (or second-type) boundary condition $-k\nabla T(x,t)|_{x=0} = q(x,t)|_{x=0}$. The