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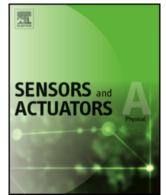

Process for integrating porous silicon with other devices

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ABSTRACT

Newly developed electrochemical etch procedures facilitate the integration of energetic porous silicon (PSi) with other devices. By confining the PSi etch process to one side of the wafer, devices on the other side of the wafer may be protected from the harsh etch conditions. This allows PSi integration with devices used for triggering or utilizing the energetic output of the PSi. The output from energetic PSi devices may be used for fusing, microthruster, MEMS actuation or other applications. Two different etch processes were developed: the sacrificial electrode process is the simplest, but it results in nonuniform PSi thickness and introduces surface topography. The anchored electrode method, which incorporates a dielectric layer, results in more controlled etch depths and allows the facile formation of patterned devices. However, in either process, a proximity effect is observed which results in deeper PSi etching closer to the electrode(s) driving the etching. A simple current divider model can be used to predict these relative etch depths. The resulting PSi burn properties have been characterized and are similar to those obtained with the previous process.

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1. Introduction

There is great interest in porous silicon (PSi) for a diverse range of applications including chem/biosensors [1–5], lithium battery anodes [6,7], radio frequeny devices [8], and solar cells [9] as well as for energetic devices [10–12]. Here, we expand on previous work describing a galvanic etch processes [13–16] that facilitates the integration of PSi with other devices. It is the aggressive concentrated hydrofluoric acid (HF)-based PSi etch solution that makes such integration difficult as it will damage other devices on the wafer. The new process, where the metal electrode and the Si to be etched are on the same side of the wafer, allows devices on the other side of the wafer to be protected during the etching. This is important as it provides significantly more flexibility for integrating PSi with other devices on the wafer or chip.

PSi is most commonly formed by anodic etching of a silicon (Si) wafer in a high concentration HF etch solution [17]. We have focused on using a galvanic etch, which is a simplified etch procedure that does not require a power supply or wires to the wafer. In this approach, a metal, typically platinum (Pt), is deposited on one side of the Si wafer, and the wafer is immersed in an HF, hydrogen peroxide (H_2O_2), and ethanol etch solution. The H_2O_2 is reduced at the catalytic metal surface injecting electron-hole (h+) charge carriers into the metal/wafer. These h + charge carriers traverse the wafer to the other side where they drive an electrochemical etching of the Si by the HF acid to produce nanoporous Si [13–15]. In this galvanic etch process, the H_2O_2 concentration and the catalytic Pt electrode area control the electrochemical etch current, without any external instrumentation. This etch current, together with the area of Si being etched, determines the etch current density which controls the etch rate as well as contributing to the resultant PSi properties [12,18–20]. If the etch current density becomes too large, the etch will no longer produce PSi but will etch all of the Si away instead (as it enters the electropolishing regime) [21]. Two same-side electrode approaches have been investigated here. In the first approach, Pt electrodes are deposited onto the Si wafer to be etched with no intervening etch resistant layer. This approach is termed the sacrificial electrode approach since the PSi etch removes the Si beneath the electrodes, eventually releasing the electrodes from the wafer. In the second approach, termed the anchored electrode approach, the electrodes are deposited on top of a silicon nitride (Si_3N_4) layer which is patterned to expose the underlying Si to be etched, and to allow electrical contact between the electrodes and the Si substrate.

It should be noted that the galvanic etch approach used here is different from metal-assisted chemical etching (MACE) of PSi. In galvanic or anodic etching, the metal electrodes are used to inject charge carriers (holes) into the Si. The carriers are then free to diffuse to etch sites, which may be at a distance from the electrodes, where pores are etched into the Si. In the MACE of PSi, noble metal

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particles are deposited onto a Si surface where they produce localized etching of pores into the Si which are similar in size to the particles. While MACE has a very rich chemistry that enables a wide range of nanostructures to be formed [22,23], it would require significant process optimization to achieve high porosity (~70%) microporous Si (~3 nm pores) with uniformly over 10's of microns in depth. These properties are needed for achieving the highest burn-rates which are desirable for many energetic PSi applications [12,24]. This is why the galvanic etch approach has been used here, although anodic etching would work as well.

2. Experimental

P-type (0.01–10 Ω) Si wafers were used here as they produce nanoporous Si suitable for energetic applications. These wafers were purchased from Rogue Valley Microdevices with 500 nm of Si_3N_4 on both sides. For sacrificial electrodes, the Si_3N_4 is removed from one side of the wafer. For anchored electrodes, photolithographically defined windows are etched through the Si_3N_4 to expose Si areas for etching and for electrical contact between the Pt electrode and the wafer. The Si_3N_4 etches are performed using a Unaxis VLR 700 reactive ion etch system.

After the Si_3N_4 has been removed or patterned as desired, any native oxide is removed with a 2 min 6:1 H_2O:HF etch followed by sputter cleaning for 30 s in a Unaxis Clusterline 200 sputter deposition system. Without breaking vacuum, the wafer is then transferred to a Pt sputter chamber where 170 nm of Pt is deposited at 250 °C. The resulting Pt layer is patterned using photolithography and an ion mill etch system (4Wave Inc. model 4W-PSIBE). In order to measure the combustion rates of the PSi, bridge wires were photolithographically deposited onto the wafers, prior to the PSi etching, using a lift-off approach with 20 nm Cr/100 nm Pt/380 nm Au deposited using a CHA Industries e-beam evaporator. The bridge wires narrow to 20 μm for 100 μm to form the active region. These bridge wires are used to electrically ignite the porous silicon samples for combustion tests, while simultaneously triggering recording with a high-speed camera. The resulting wafers, which have patterned Pt electrodes, exposed Si, and integrated bridge wires are then diced with a wafer saw. The individual die have a 5 min cure, two-part silicone deposited on their edges to keep the exposed Si at the die edges from etching.

The etch set-up is very simple and requires no power supply or additional electrodes as the Si and Pt surfaces on the die and the etch solution form the complete electrochemical system [13,14]. Given the self-contained nature of the electrochemical cell, etch currents are not measureable and are only controlled by the amount of H_2O_2 and the area of the Pt electrode that catalyzes the reduction of the H_2O_2 which injects holes (the etch current) into the Si substrate. The die are suspended in a plastic beaker of etch solution using plastic clamping forceps. The etch solution is stirred using a magnetic stir bar to ensure uniform etch species concentrations. The die are electrochemically etched for a few to tens of minutes with a concentrated HF, absolute ethanol, and H_2O_2 mixture. The ethanol reduces the viscosity/surface tension of the etch solution so that it can penetrate into the nanometer scale pores being formed. A typical etch composition is 3:1 HF:ethanol with 2.5% H_2O_2.

The etch depths were characterized using scanning electron microscope (SEM) cross-section micrographs obtained with a Hitachi S4500 SEM. Etch depth measurements were also made, after removing the PSi with a 1 M sodium hydroxide (NaOH) with 20% ethanol etch [25], using a Wyko NT1100 optical profilometer. The optical profilometer method, though less accurate due to the NaOH etch roughness, was used for Figs. 4 and 5 as it was not possible to controllably cleave these samples in enough places to obtain this data.

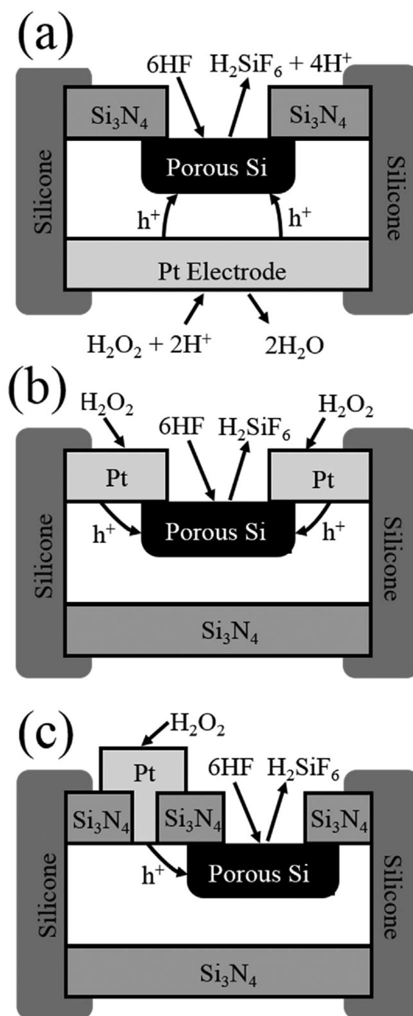

Fig. 1. Drawings depicting (a) the original backside electrode process, (b) the sacrificial electrode process, and (c) the anchored electrode process.

In order to burn the PSi, an oxidizer is applied to the PSi in the form of a 3.2 M sodium perchlorate in methanol solution drop cast by hand using a micropipette. After drying under nitrogen for 30 min (sodium perchlorate is very hygroscopic), the PSi is ignited by passing 10 V/1 A of current across the bridge wire or by delivery of a spark to the PSi from a probe tip connected to a battery powered spark generator. This is done while simultaneously triggering a Photron Devices Inc, high-speed camera used to measure the PSi burn rate.

3. Results

3.1. Sacrificial electrodes

The sacrificial electrode approach is the simpler of the two same-side electrode approaches as it requires only a metal (Pt) deposition and patterning process before the PSi etch. This is similar to the backside electrode process we have previously used [15], where a blanket Pt electrode is deposited on the wafer backside and the areas to be etched are masked on the front-side with a Si_3N_4 layer. Typically, the wafer is diced prior to etching and the edges of the die are protected from the etchant with silicone. This silicone also protects the blanket backside electrode edges whereas the edges of the sacrificial (front-side) electrodes are unprotected. Fig. 1a and b are drawings comparing these two etch approaches.

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